Serial EEPROM Series Standard EEPROM
WLCSP EEPROM
BU9847GUL-W (4Kbit)

●General Description
BU9847GUL-W series is a serial EEPROM of I²C BUS interface method. 1.7V single power source action and actions available at 400kHz.

●Features
- Completely conforming to the world standard I²C BUS. All controls available by 2 ports of serial clock (SCL) and serial data(SDA)
- Other devices than EEPROM can be connected to the same port, saving microcontroller port.
- Actions available at 400kHz clock (1.7V to 5.5V)
- 1.7V to 5.5V single power source action most suitable for battery use.
- Page write mode useful for initial value write at factory shipment.
- Auto erase and auto end function at data rewrite.
- Low current consumption
  - At write action (5V) : 1.2mA (Typ.)
  - At read action (5V) : 0.2mA (Typ.)
  - At standby action (5V) : 0.1μA (Typ.)
- Write mistake prevention function
  - Write (write protect) function added.
  - Write mistake prevention function at low voltage.
- Data rewrite up to 1,000,000times.
- Data kept for 40 years.
- Noise filter built in SCL / SDA terminal
- Shipment data all address FFh.

●Package W(Typ.) x D(Typ.) x H(Max.)
VCSP50L1:1.95mm x 1.06mm x 0.55mm

●Page Write

Number of pages	16Byte
Product number	BU9847GUL-W

●BU9847GUL-W

Capacity	Bit format	Type	Power source voltage	VCSP50L1
4Kbit	512×8	BU9847GUL-W	1.7V to 5.5V	●

●Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit	Remarks
Impressed voltage	Vcc	-0.3 to +6.5	V	
Permissible dissipation	Pd	220	mW	When using at Ta=25℃ or higher, 2.2mW to be reduced per 1℃
Storage temperature range	Tstg	-65 to 125	℃	
Operating temperature range	Topr	-40 to 85	℃	
Terminal voltage	-	-0.3 to Vcc+1.0	V	

●Memory cell characteristics (Ta=25°C, V_{CC} =1.7V to 5.5V)

Parameter	Limits			Unit
	Min	Typ.	Max	
Number of data rewrite times *1	1,000,000	-	-	Times
Data hold years *1	40	-	-	Years

Shipment data all address FFh
*1 Not 100% TESTED

●**Recommended Operating Ratings**

Parameter	Symbol	Ratings	Unit
Power source voltage	V_{CC}	1.7 to 5.5	V
Input voltage	Vin	0 to V_{CC}	

●**Electrical characteristics**

(Unless otherwise specified, Ta=-40℃ to +85°C, Vcc=1.7V to 5.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
“HIGH” input voltage1	V_{IH1}	$0.7V_{CC}$	-	V_{CC}+1.0	V	2.5V≦V_{CC}≦5.5V
“LOW” Input voltage1	V_{IL1}	-0.3	-	$0.3V_{CC}$	V	2.5V≦V_{CC}≦5.5V
“HIGH” input voltage2	V_{IH2}	$0.8V_{CC}$	-	V_{CC}+1.0	V	1.8V≦V_{CC}<2.5V
“LOW” input voltage2	V_{IL2}	-0.3	-	$0.2V_{CC}$	V	1.8V≦V_{CC}<2.5V
“HIGH” input voltage3	V_{IH3}	$0.9V_{CC}$	-	V_{CC}+1.0	V	1.7V≦V_{CC}<1.8V
“LOW” input voltage3	V_{IL3}	-0.3	-	$0.1V_{CC}$	V	1.7V≦V_{CC}<1.8V
“LOW” output voltage1	V_{OL1}	-	-	0.4	V	I_{OL}=3.0mA, 2.5V≦V_{CC}≦5.5V, (SDA)
“LOW output voltage2	V_{OL2}	-	-	0.2	V	I_{OL}=0.7mA, 1.7V≦V_{CC}≦2.5V, (SDA)
Input leak current	I_{LI}	-1	-	1	μA	V_{IN}=0V to V_{CC}
Output leak current	I_{LO}	-1	-	1	μA	V_{OUT}=0V to V_{CC}(SDA)
Current consumption at action	I_{CC1}	-	-	2.0	mA	V_{CC}=5.5V, fSCL =400kHz, tWR=5ms, Byte write, Page write
	I_{CC2}	-	-	0.5	mA	V_{CC}=5.5V, fSCL =400kHz Random read, Current read, sequential read
Standby current	I_{SB}	-	-	2.0	μA	V_{CC}=5.5V, SDA·SCL=V_{CC}, A2=GND, WP=GND

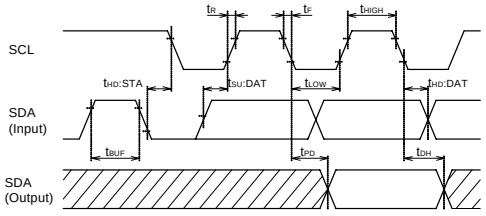
●**Action timing characteristics**

(Unless otherwise specified, Ta=-40℃ to +85°C、V_{CC}=1.7V to 5.5V)

Parameter	Symbol	FAST-MODE 1.7V≦V_{CC}≦5.5V			Unit
		Min.	Typ.	Max.	
SCL frequency	fSCL	-	-	400	kHz
Data clock “HIGH“ time	tHIGH	0.6	-	-	μs
Data clock “LOW“ time	tLOW	1.2	-	-	μs
SDA, SCL rise time *1	tR	-	-	0.3	μs
SDA< SCL fall time *1	tF	-	-	0.3	μs
Start condition hold time	tHD:STA	0.6	-	-	μs
Start condition setup time	tSU:STA	0.6	-	-	μs
Input data hold time	tHD:DAT	0	-	-	ns
Input data setup time	tSU:DAT	100	-	-	ns
Output data delay time	tPD	0.1	-	0.9	μs
Output data hold time	tDH	0.1	-	-	μs
Stop condition setup time	tSU:STO	0.6	-	-	μs
Bus release time before transfer start	tBUF	1.2	-	-	μs
Internal write cycle time	tWR	-	-	5	ms
Noise removal valid period (SDA, SCL terminal)	tI	-	-	0.1	μs
WP hold time	tHD:WP	0	-	-	ns
WP setup time	tSU:WP	0.1	-	-	μs
WP valid time	tHIGH:WP	1.0	-	-	μs

*1 Not 100% tested.

●Sync Data Input / Output Timing



○Input read at the rise edge of SCL
○Data output in sync with the fall of SCL

Figure 1-(a) Sync data input / output timing

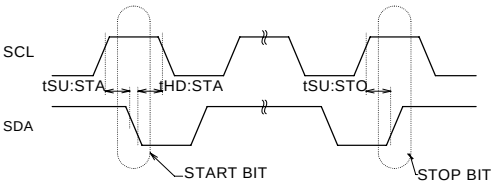


Figure 1-(b) Start – stop bit timing

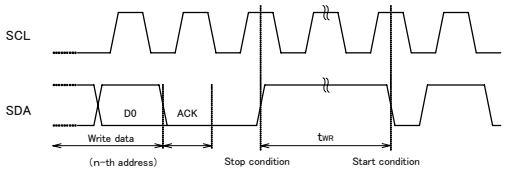


Figure 1-(c) Write cycle timing

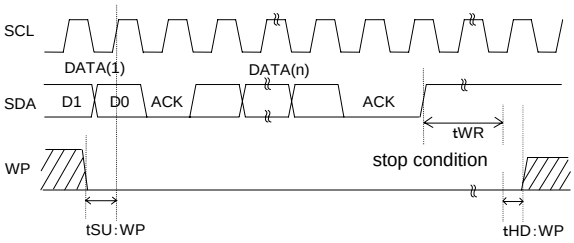


Figure 1-(d) WP timing at write execution

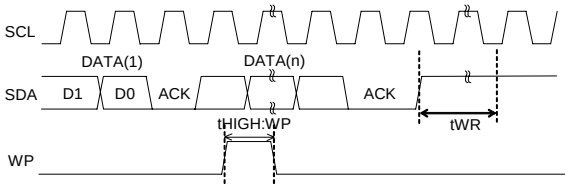
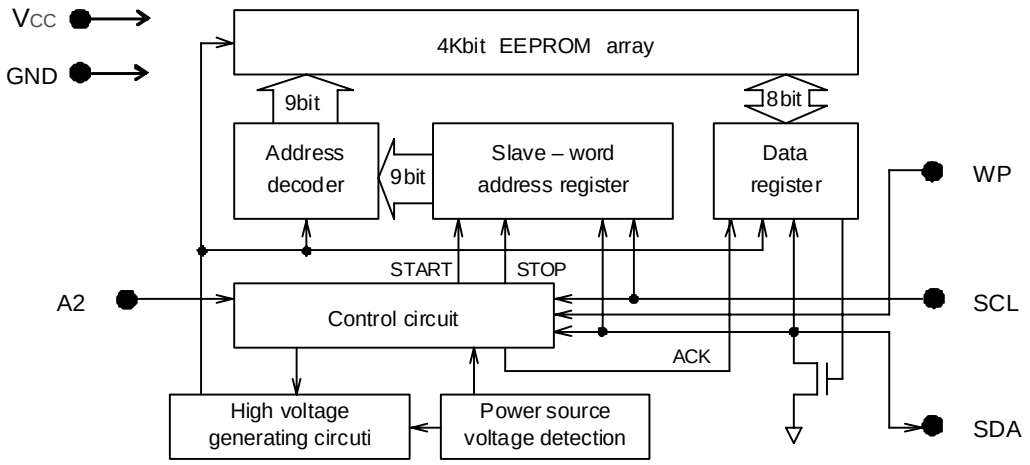


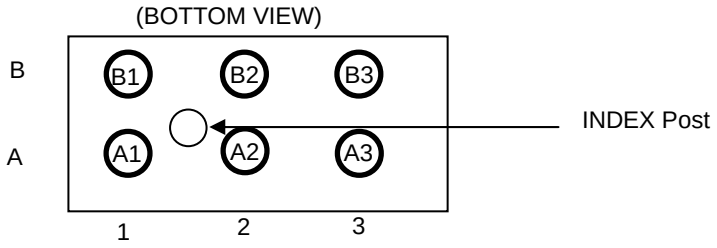
Figure 1-(e) WP timing at write cancel

○At write execution, in the area from the DO taken clock rise of the first DATA (1), to tWR, set WP=”LOW”
○By setting WP “HIGH” in the area, write can be cancelled.
When it is set WP=”HIGH” during tWR, write is forcibly ended, and data of address under access is not guaranteed, therefore write it once again.

●**Block Diagram**



●**Pin Configuration**



●**Pin Descriptions**

Land No.	Terminal name	Input/ Output	Function
B3	A2	Input	Slave address setting terminal
B2	GND	-	Reference voltage of al input / output, 0V
B1	SDA	Input/Output	Slave and word address, Serial data input serial data output.
A3	Vcc	-	Connect the power source.
A2	WP	Input	Write protect terminal
A1	SCL	Input	Serial clock input

●**Typical Performance Curves**
(The following values are Typ. ones.)

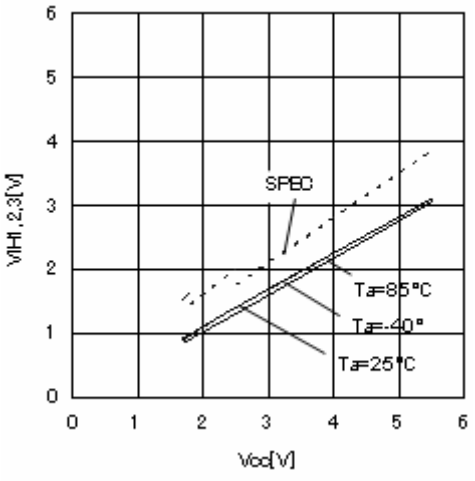


Figure 2. H input voltage VIH1,2,3
(A2,SCL,SDA,WP)

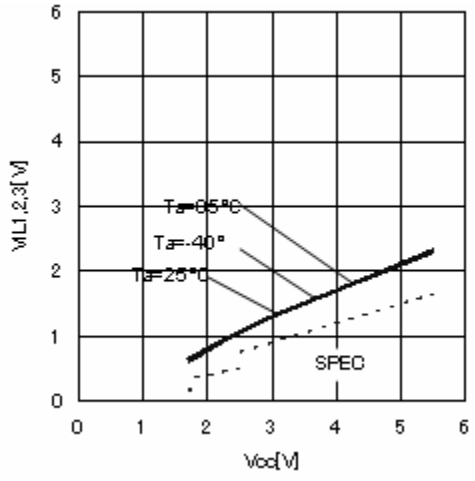


Figure 3. L input voltage VIL1,2,3
(A2,SCL,SDA,WP)

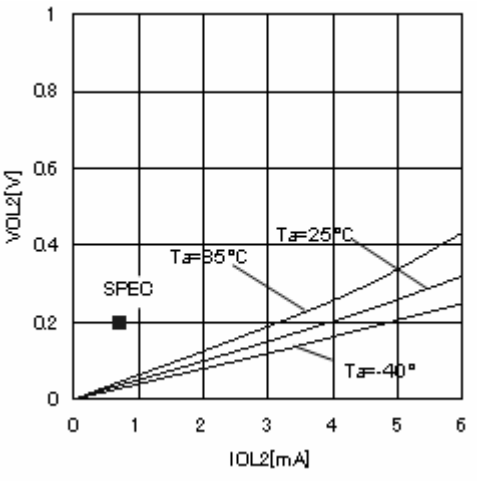


Figure 4. L output voltage VOL2-IOL2
(VCC=1.7V)

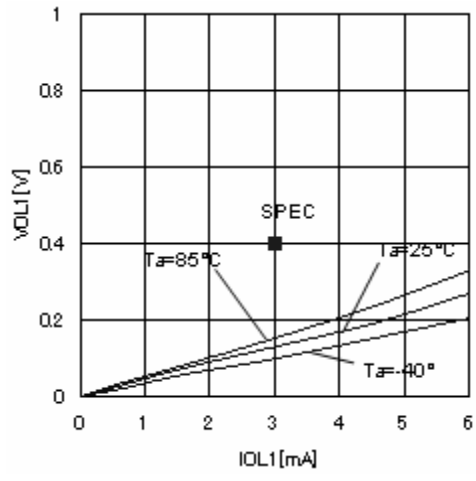


Figure 5. L input voltage
VOL1-IOL1 (Vcc=2.5V)

●**Typical Performance Curves - Continued**

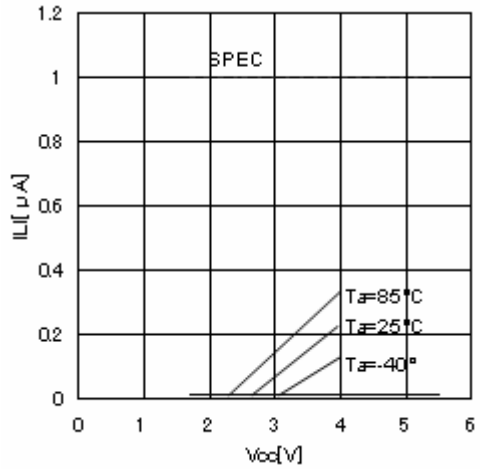


Figure 6. Input leak current
ILI(A2,SCL, WP)

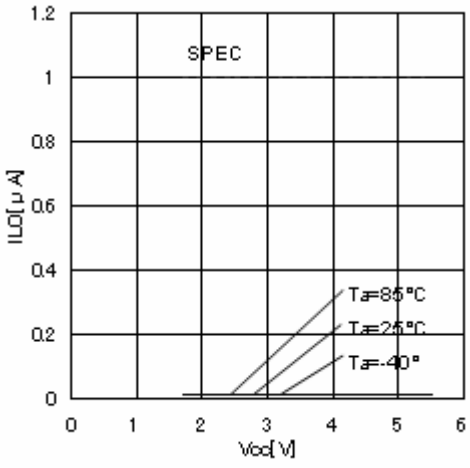


Figure 7. Output leak current
ILO (SDA)

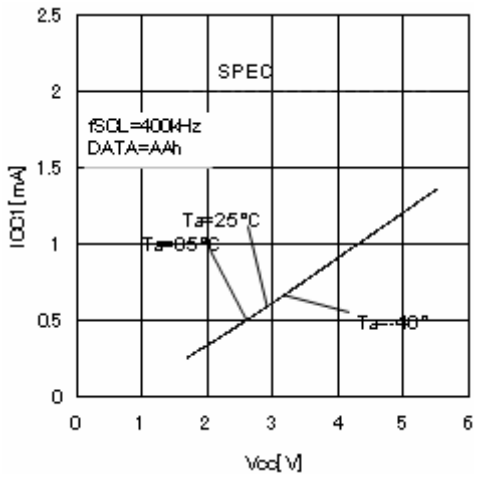


Figure 8. Consumption current
at write action Icc1 (fSCL=400kHz)

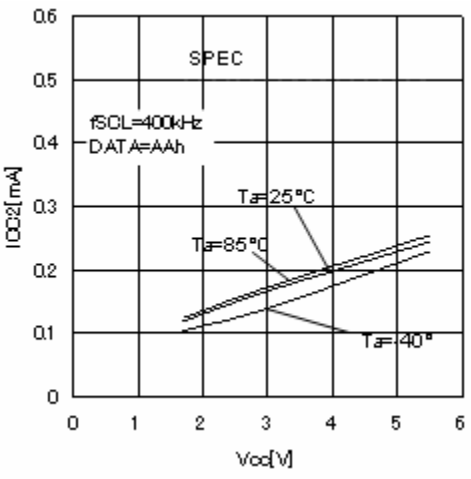


Figure 9. Consumption current
at write action Icc2 (fSCL=400kHz)

●**Typical Performance Curves - Continued**

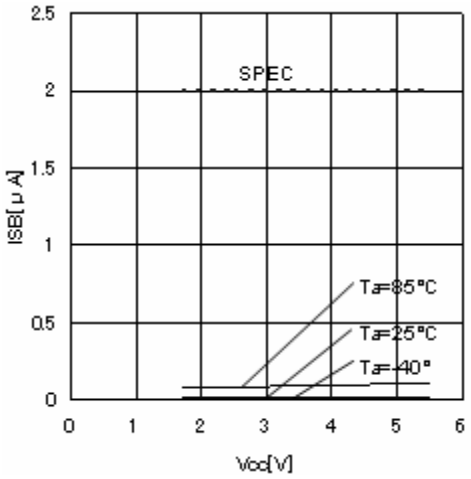


Figure 10. Standby current
I_{SB}

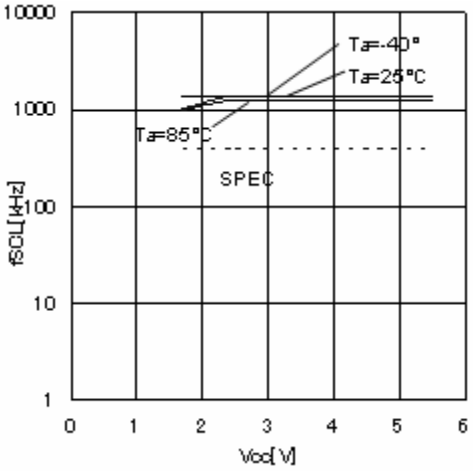


Figure 11. SCL frequency
f_{SCL}

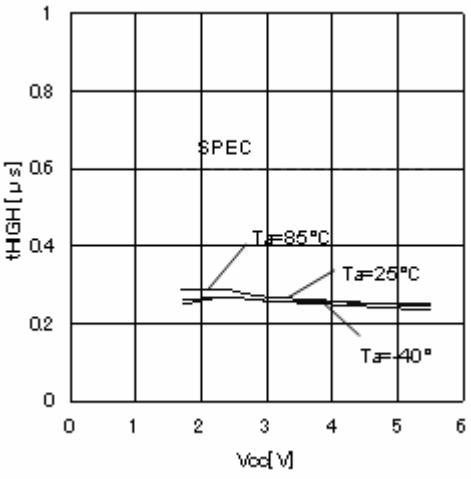


Figure 12. Data clock “H” time
tHIGH

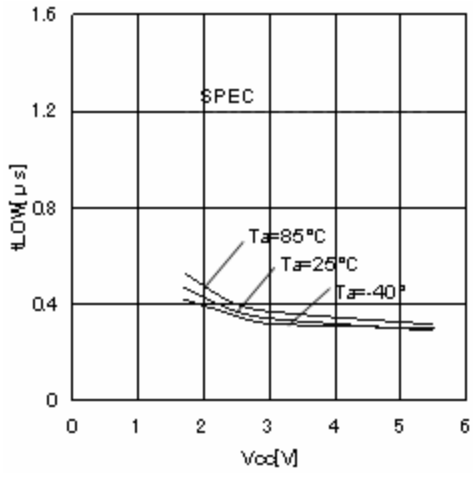


Figure 13. Data clock “L” time
tLOW

●**Typical Performance Curves - Continued**

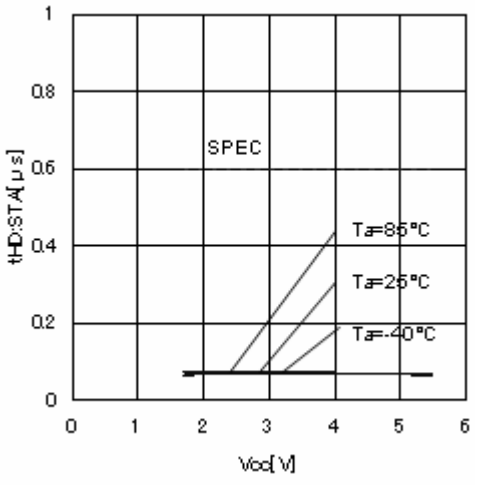


Figure 14. Start condition hold time
tHD:STA

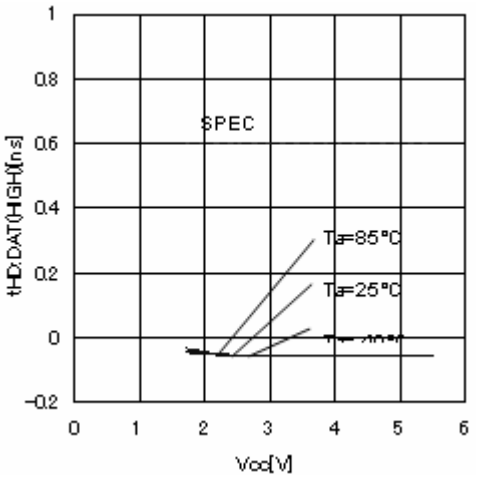


Figure 15. Start condition setup time
tSU:STA

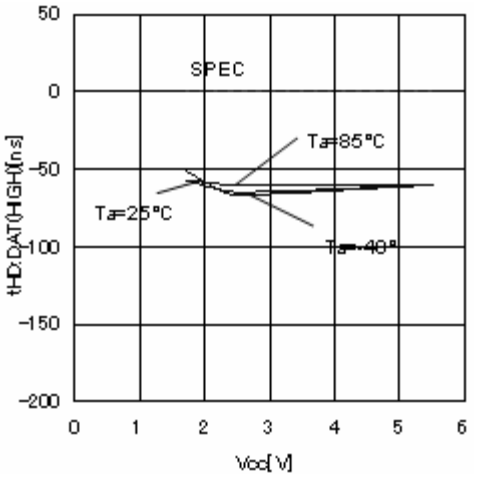


Figure 16. Input data hold time
tHD:DAT

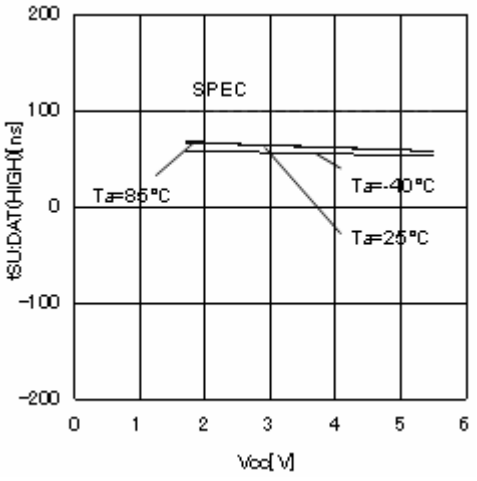


Figure 17. Input data setup time
tSU:DAT

●**Typical Performance Curves - Continued**

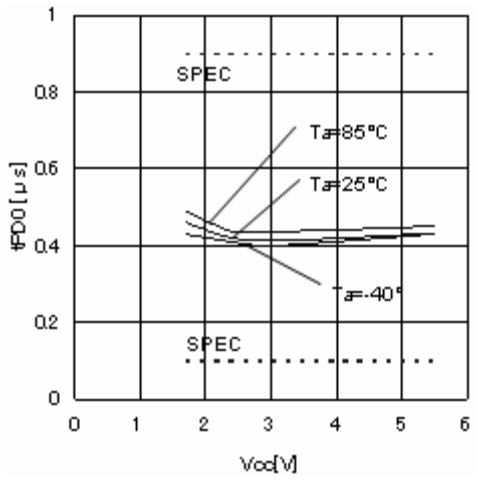


Figure 18. Output data delay time tPD0

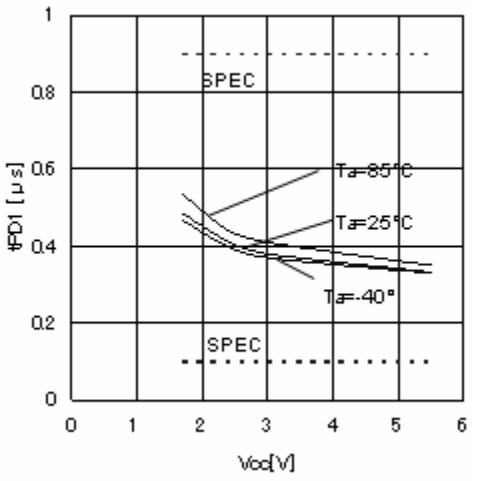


Figure 19. Output data delay time tPD1

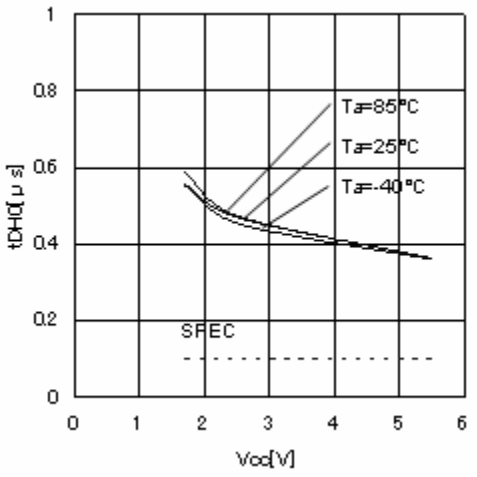


Figure 20. Output data hold time tDH1

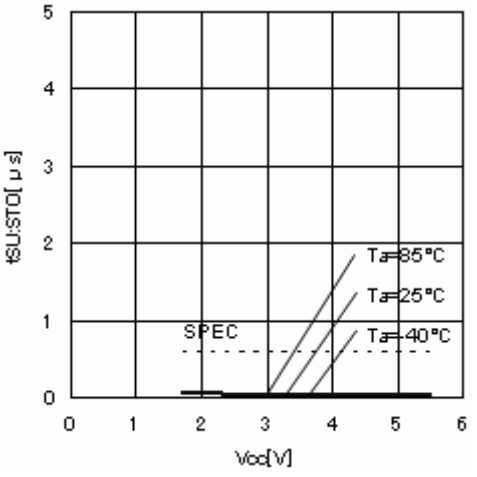


Figure 21. Stop condition setup time tSU:STO

●**Typical Performance Curves - Continued**

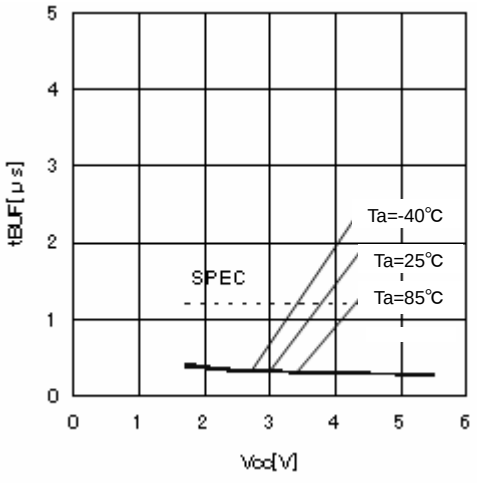


Figure 22. Bus release time before transfer start tBUF

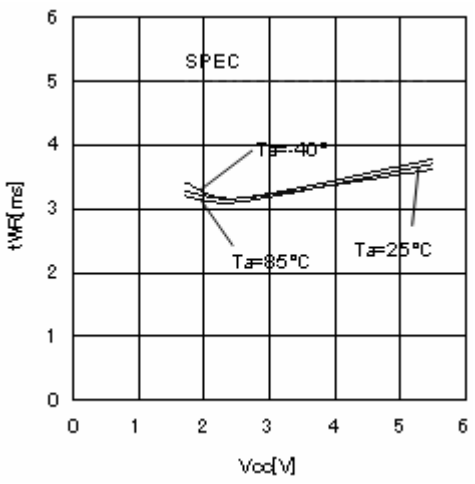


Figure 23. Internal write cycle time tWR

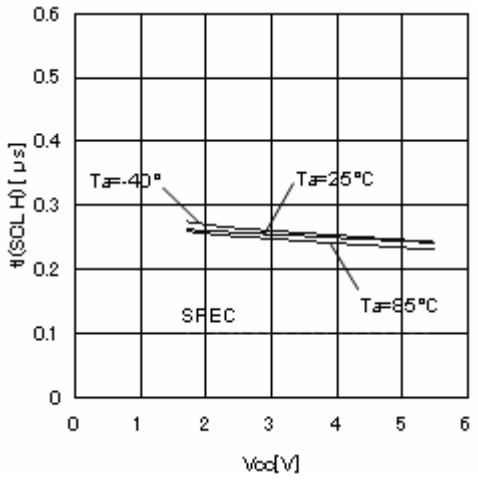


Figure 24. Noise removal time tI (SCL H)

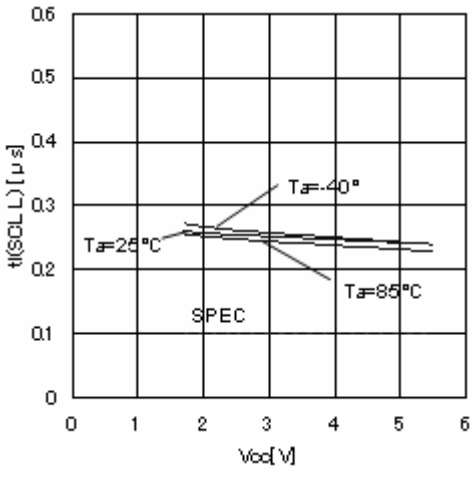


Figure 25. Noise removal time tI (SCL L)

●**Typical Performance Curves - Continued**

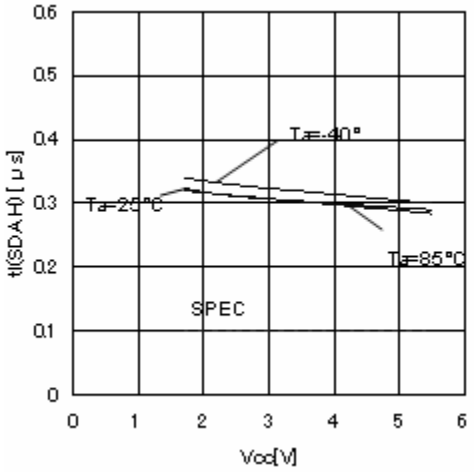


Figure 26. Noise removal time
tI (SDA H)

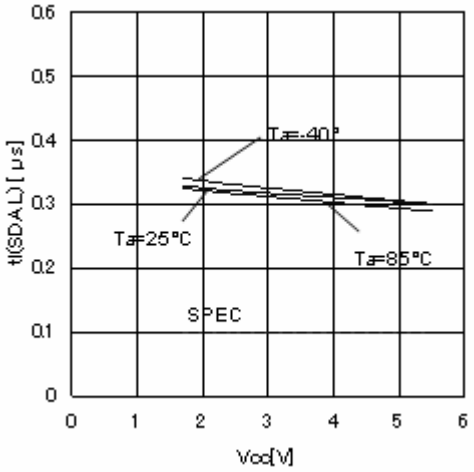


Figure 27. Noise removal time
tI (SDA L)

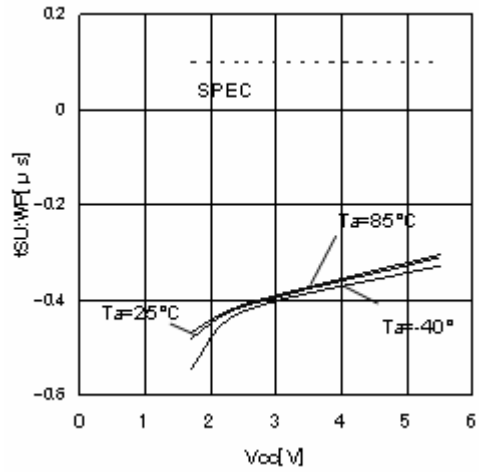


Figure 28. WP setup time
tSU:WP

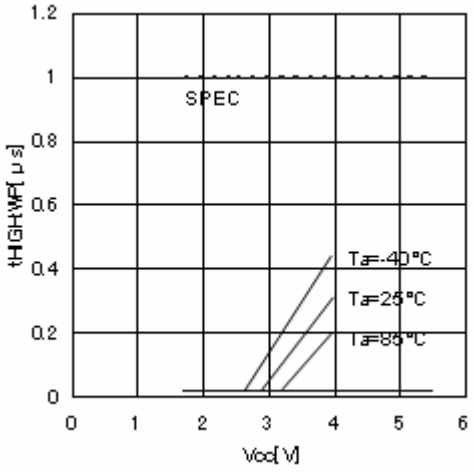


Figure 29. WP valid time
tHIGH: WP

●I²C BUS communication

○I²C BUS data communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte.

I²C BUS carries out data transmission with plural devices connected by 2 communication lines of serial data (SDA) and serial clock (SCL).

Among devices, there are “master” that generates clock and control communication start and end, and “slave” that is controlled by addresses peculiar to devices.

EEPROM becomes “slave”. And the device that outputs data to bys during data communication is called “transmitter”, and the device that receives data is called “receiver “.

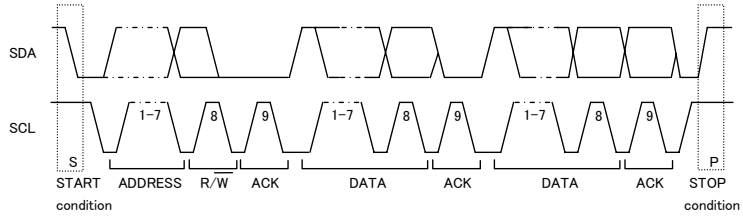


Figure 30. Data transfer timing

○Start condition (start bit recognition)

- Before executing each command, start condition (start bit) where SDA goes from “HIGH” down to “LOW” when SCL is “HIGH” is necessary.
- This IC always detects whether SDA and SCL are in start condition (start bit) of not, therefore, unless this condition is satisfied, any command is executed.

○Stop condition (stop bit recognition)

- Each command can be ended by SDA rising from “LOW” to “HIGH” when stop condition (stop bit), namely, SCL is “HIGH”.

○Acknowledge (ACK) signal

- This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master and slave, the device (µ-COM at slave address input of write command, read command, and this IC at data output of read command) at the transmitter (sending) side releases the bus after output of 8bit data.
- This device (this IC at slave address input of write command , read command , and µ-COM at data output of read command) at the receiver (receiving) side sets SDA “LOW” during 9 clock cycles, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
- This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) “LOW”.
- Each write action outputs acknowledge signal (ACK signal) “LOW”, at receiving 8bit data (word address and write data).
- Each read action outputs 8bit data (read data), and detects acknowledge signal (ACK signal) “LOW”.
- When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (µ-COM) side, this IC continues data output. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, and recognizes stop condition (stop bit), and ends read action.
  And this IC gets in standby status.

○Device addressing

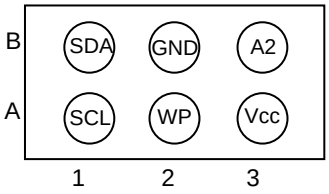
- Output slave address after start condition from master.
- The significant 4 bits of slave address are used for recognizing a device type.
  The device code of this IC is fixed to “1010”.
- Next slave addressed (A2 --- device address) are for selecting devices, and plural ones can be used on a same bus according to the number of device addresses.
- The most insignificant bit (R / $\overline{W}$ --- READ / WRITE) of slave address is used for designating write or read action, and is as shown below.

Setting R / $\overline{W}$ to 0 --- write (setting 0 to word address setting of random read)

Setting R / $\overline{W}$ to 1 --- read

Type	Slave address	Maximum number of connected buses
BU9847GUL-W	1 0 1 0 A2 0 PS R / $\overline{W}$	2

PS is page select bits.



●Command

○Write cycle

・Arbitrary data is written to EEPROM. When to write only 1 byte, byte write is normally used, and when to write continuous data of 2 bytes or more, simultaneous write is possible by page write cycle.

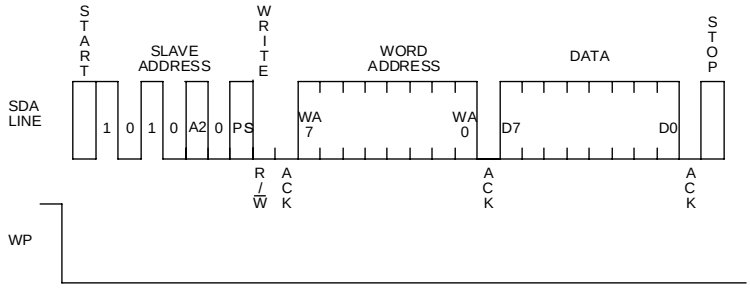


Figure 31. Byte write cycle

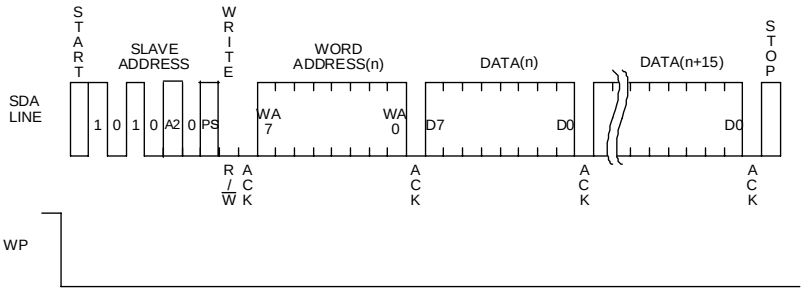


Figure 32. Page write cycle

・Data is written to the address designated by word address (n-th address).
・By issuing stop bit after 8bit data input, write to memory cell inside starts.
・When internal write is started, command is not accepted for tWR (5ms at maximum).
・By page write cycle, the following can be written in bulk. Up to 16 bytes.
And when data of the maximum bytes or higher is sent, data from the first byte is overwritten.
(Refer to “Internal address increment” in Page 14.)
・As for page write cycle of BU9847GUL-W, after page select bit (PS) of slave address is designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 4 bits is incremented internally, and data up to 16 bytes can be written.

Note)

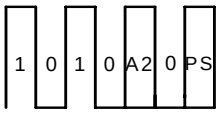


Figure 33. Difference of slave address of each type

○Notes on write cycle continuous input

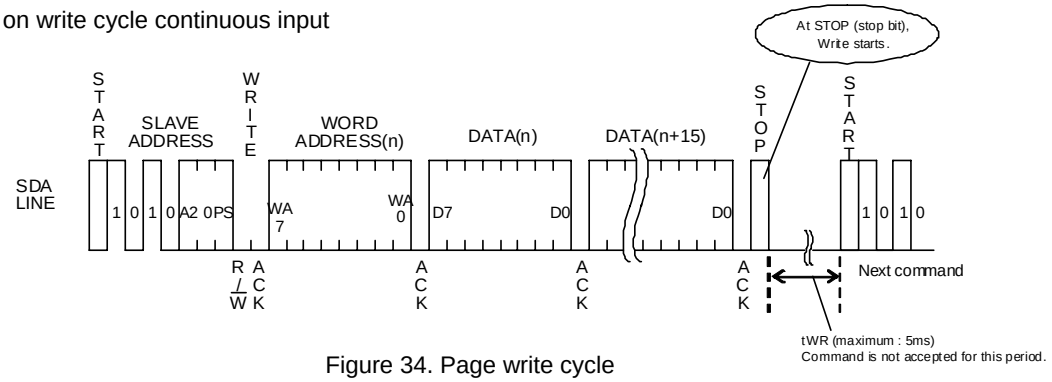


Figure 34. Page write cycle

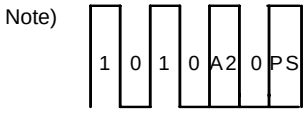


Figure 35. Difference of each type of slave address

○Notes on page write cycle

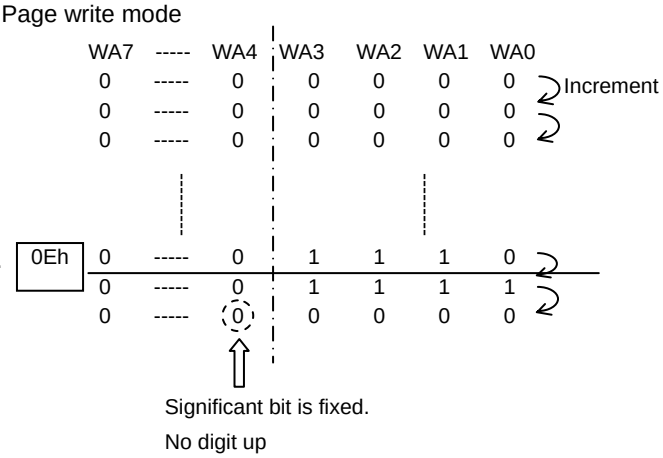
List of numbers of page write

Number of Pages	16Byte
Product number	BU9847GUL-W

The above numbers are maximum bytes for respective types.
Any types below these can be written.

1page = 16 bytes, but the page write cycle write time is 5ms at maximum for 16byte bulk write.
It does not stand 5ms at maximum x 16 bytes = 80ms (Max.).

○Internal address increment
Page write mode



For example, when it is started from address 0Eh, therefore, increment is made as below,
0Eh→0Fh→00h→01h ---, which please note.
*0Eh --- 0E in hexadecimal, therefore, 00001110 becomes a binary number.

○Write protect terminal (WP)

・Write protect function
When WP terminal is set Vcc (H level), data rewrite of all addresses is prohibited. When it is set GND (L level), data rewrite of all addresses is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not use it open.
At extremely low voltage at power ON/OFF, by setting the WP terminal “H”, mistake write can be prevented.
During tWR, set the WP terminal always to “L”. If it is set “H”, write is forcibly terminated.

●Command

○Read cycle

Data of EEPROM is read. In read cycle, there are random read cycle and current read cycle.
Random read cycle is a command to read data by designating address, and is used generally.
Current read cycle is a command to read data of internal address register without designating address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available, and the next address data next address data can be read in succession.

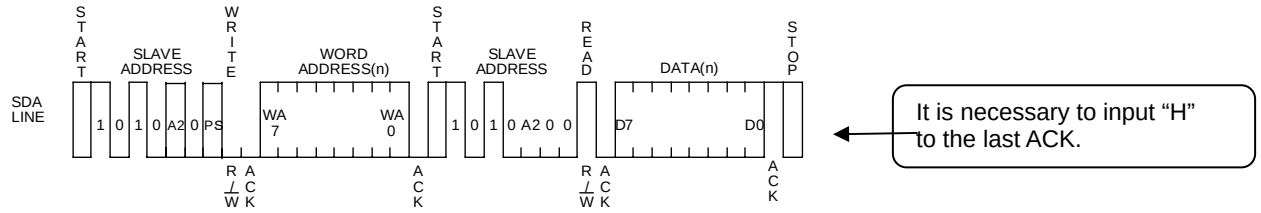


Figure 36. Random Read cycle

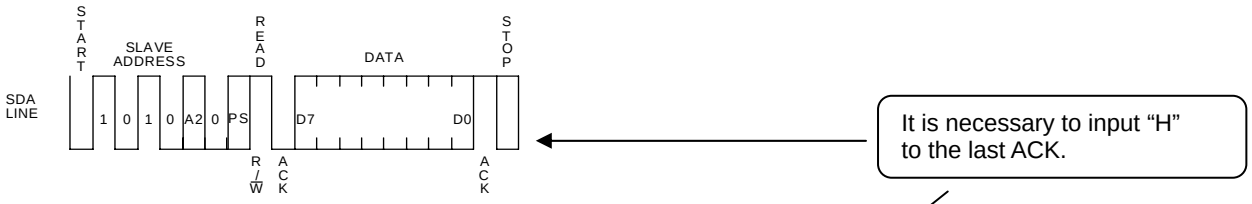


Figure 37. Current read cycle

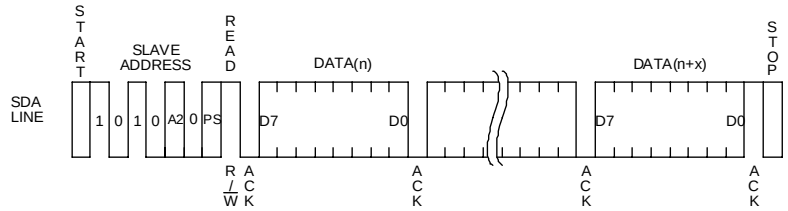


Figure 38. Sequential read cycle

- In random read cycle, data of designated word address can be read.
- When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n-th) address, i.e., data of the (n+1)-th address is output.
- When ACK signal “LOW” after D0 is detected, and stop condition is not sent from the master (μ-COM) side, the next address data can be read in succession.
- Read cycle is ended by stop condition where “H” is input to ACK signal after D0 and SDA signal is started at SCL signal “H”.
- When “H” is not input to ACK signal after D0, sequential read gets in, and the next data is output.
  Therefore, read command cycle cannot be ended. When to end read command cycle, be sure input stop condition to input “H” to ACK signal after D0, and to start SDA at SCL signal “H”.
- Sequential read is ended by stop condition where “H” is input to ACK signal after arbitrary D0 and SDA is started at SCL signal “H”.

Note)

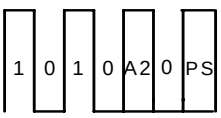


Figure 39. Difference of slave address of each type

●Software reset

Software reset is executed when to avoid malfunction after power on, and to reset during command input. Software reset has several kinds, and 3 kinds of them are shown in the figure below. (Refer to Figure 40-(a), Figure 40-(b) and Figure 40-(c).) In dummy clock input area, release the SDA bus (“H” by pull up). In dummy clock area, ACK output and read data “0” (both “L” level) may be output from EEPROM, therefore, if “H” is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

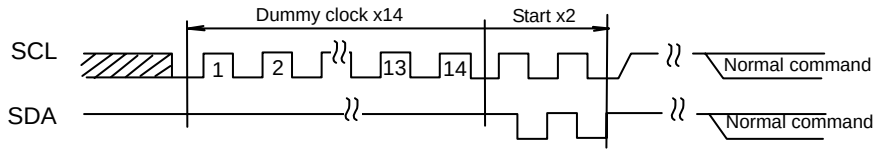


Figure 40-(a) The case of dummy clock + START + START + command input

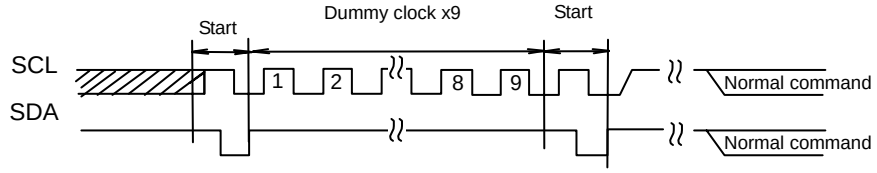


Figure 40-(b) The case of START + 9 dummy clocks + START + command input

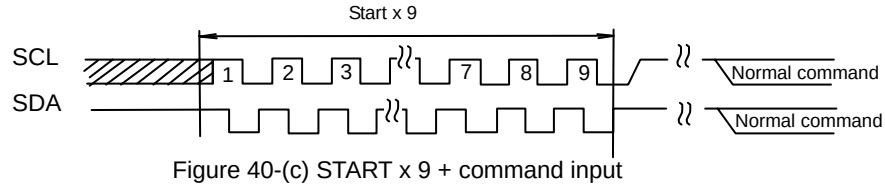


Figure 40-(c) START x 9 + command input

* Start normal command from START input.

●Acknowledge polling

During internal write execution, all input commands are ignored, therefore ACK is not sent back. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back “L”, then it means end of write action, while if it sends back “H”, it means now in writing. By use of acknowledge polling, next command can be executed without waiting for tWR=5ms.

When to write continuously, $R/\overline{W}$ = 0, when to carry out current read cycle after write, slave address $R/\overline{W}$ = 1 is sent, and if ACK signal sends back “L”, then execute word address input and data output and so forth.

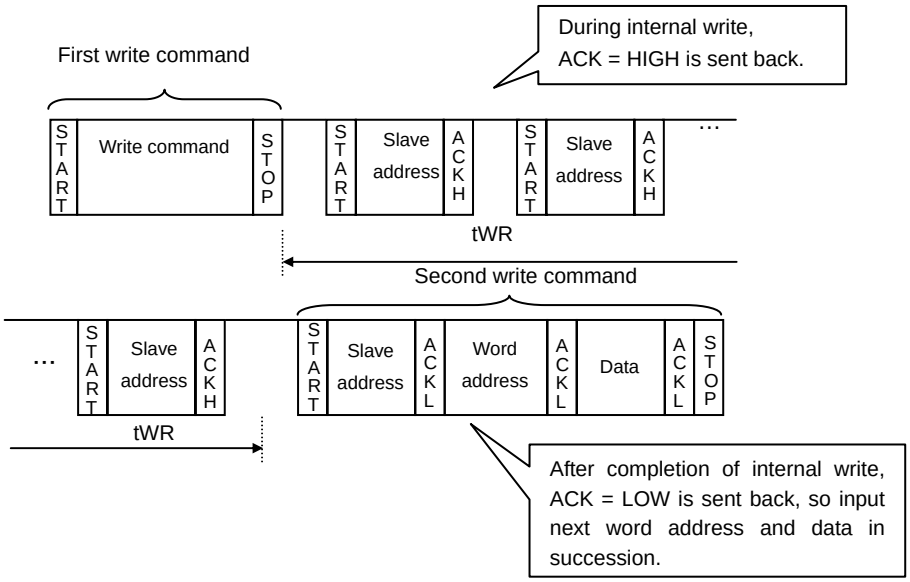


Figure 41. Case to continuously write by acknowledge polling

●WP valid timing (write cancel)

WP is usually to “H” or “L”, but when WP is used to cancel write cycle and so forth, pay attention to the following WP valid timing.
During write cycle execution, in cancel valid area, by setting WP = “H”, write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to taken in D0 of data (in page write cycle, the first byte data) is cancel invalid area.
WP input in this area becomes don’t care. Set the setup time to rise of D0 taken SCL 100ns or more. The area from the rise of SCL to take in D0 to the end of internal automatic write (tWR) is cancel valid area. And, when it is set WP = “H” during tWR, write is ended forcibly, data of address under access is not guaranteed, therefore, write it once again. (Refer to Figure 42.) After execution of forced end by WP, standby status gets in, so there is no need to wait for tWR (5ms at maximum).

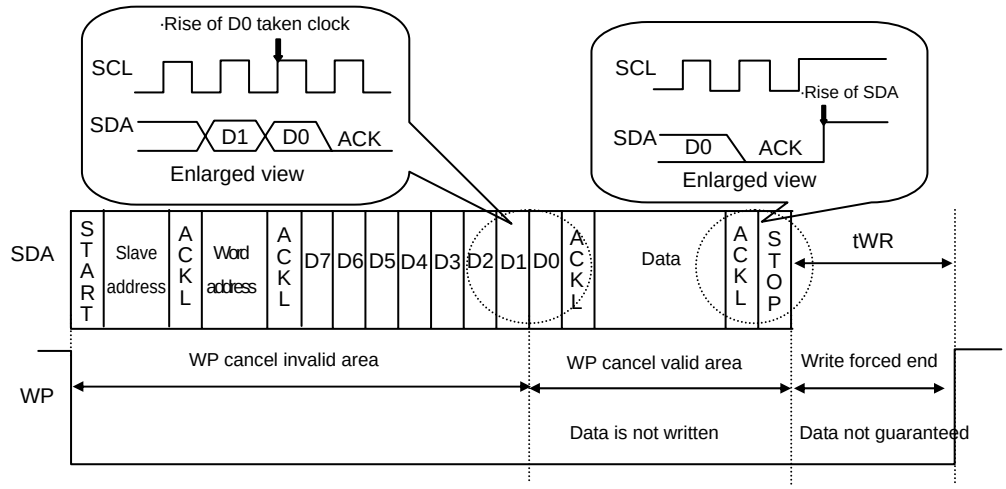


Figure 42. WP valid timing

●Command cancel by start condition and stop condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Refer to Figure 43.)
However, in ACK output area and during data read, SDA bus may output “L”, and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. and when command is cancelled by start, stop condition, during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined, therefore, it is not possible to carry out current read cycle in succession. When to carry out read cycle in succession, carry out random read cycle.

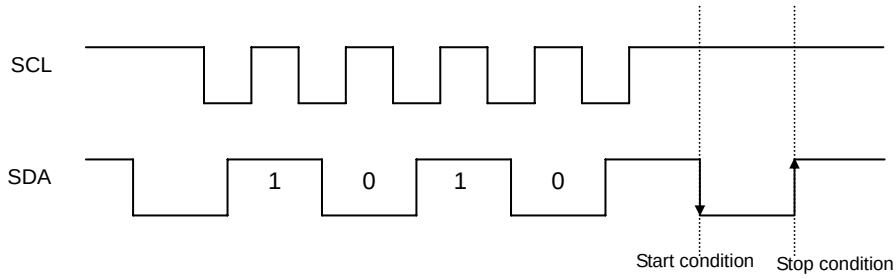


Figure 43. Case of cancel by start, stop condition during slave address input

●I/O peripheral circuit

○Pull up resistance of SDA terminal

SDA is NMOS open drain, so requires pull up resistance. As for this resistance value (R_{PU}), select an appropriate value to this resistance value from microcontroller V_{IL}, I_L, and V_{OL}-I_{OL} characteristics of this IC. If R_{PU} is large, action frequency is limited. The smaller the R_{PU}, the larger the consumption current at action.

○Maximum value of R_{PU}

The maximum value of R_{PU} is determined by the following factors.

(1) SDA rise time to be determined by the capacity (CBUS) of bus line of R_{PU} and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

(2) The bus electric potential Ⓐ to be determined by input leak total (I_L) of device connected to bus at output of "H" to SDA bus and R_{PU} should sufficiently secure the input "H" level (V_{IH}) of microcontroller and EEPROM including recommended noise margin 0.2Vcc.

$$V_{CC}-I_L R_{PU}-0.2\,V_{CC} \geqq V_{IH}$$

$$\therefore \quad R_{PU} \leqq \frac{0.8V_{CC}-V_{IH}}{I_L}$$

Ex.) When V_{CC} =3V, I_L=10μA, V_{IH}=0.7 Vcc

from (2)

$$R_{PU} \leqq \frac{0.8\times3-0.7\times3}{10\times10^{-6}}$$

$$\leqq 300\ [k\Omega]$$

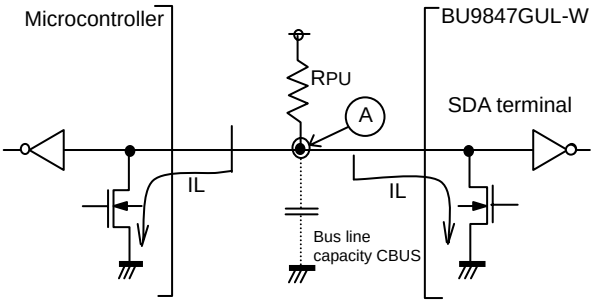


Figure 44. I/O circuit diagram

○Minimum value of R_{PU}

The minimum value of R_{PU} is determined by the following factors.

(1) When IC outputs LOW, it should be satisfied that V_{OLMAX} = 0.4V and I_{OLMAX} = 3mA.

$$\frac{V_{CC}-V_{OL}}{R_{PU}} \leqq I_{OL} \qquad \therefore \quad R_{PU} \geqq \frac{V_{CC}-V_{OL}}{I_{OL}}$$

(2) V_{OLMAX} = 0.4V should secure the input "L" level (VIL) of microcontroller and EEPROM including recommended noise margin 0.1V_{CC}.

$$V_{OLMAX} \leqq V_{IL} - 0.1V_{CC}$$

Ex.) When V_{CC} = 3V, V_{OL} = 0.4V, I_{OL} = 3mA, microcontroller, EEPROM V_{IL} = 0.3V_{CC}

From (1), $\therefore R_{PU} \geqq \dfrac{3-0.4}{3 \times 10^{-3}}$

$\geqq 867[\Omega]$

And V_{OL} = 0.4[V]

V_{IL} = 0.3 x 3

=0.9 [V]

Therefore, the condition (2) is satisfied.

○Pull up resistance of SCL terminal

When SCL control is made at CMOS output port, there is no need, but in the case there is timing where SCL becomes "Hi-Z", add a pull up resistance. As for the pull up resistance, one of several kΩ to several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.

●A2, WP process

○Process of device address terminals (A2)

Check whether the set device address coincides with device address input sent from the master side or not, and select one among plural devices connected to a same bus. Connect this terminal to pull up of pull down, or V_{CC} or GND.

○Process of WP terminal

WP terminal is the terminal that prohibits and permits write in hardware manner. In "H" status, only READ is available and WRITE of all addresses is prohibited. In the case of "L", both are available. In the case to use it as an ROM, it is recommended to connect it to pull up or V_{CC}. In the case to use both READ and WRITE, control WP terminal or connect it to pull down or GND.

●Cautions on microcontroller connection

○Rs

In I^2C BUS, it is recommended that SDA port is of open drain input / output. However, when to use COMS input / output of tri state to SDA port, insert a series resistance Rs between the pull up resistance R_{PU} and the SDA terminal of EEPROM. This controls over protection of SDA terminal against surge. Therefore, even when SDA port is open drain input / output, Rs can be used.

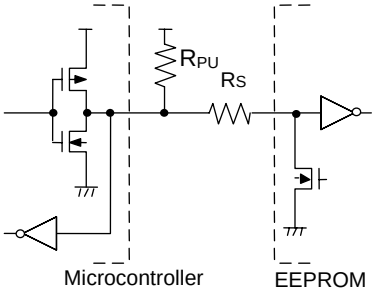


Figure 45. I/O circuit diagram

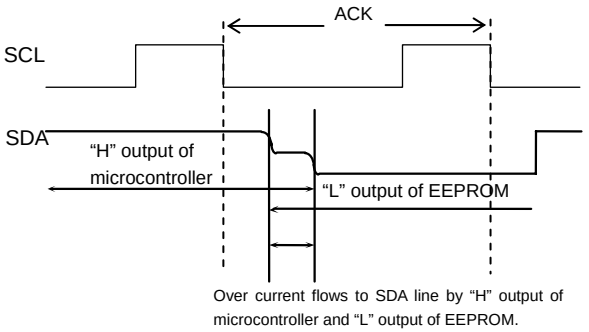


Figure 46. Input / output collision timing

○Maximum value of Rs

The maximum value of Rs is determined by the following relations.

(1) SDA rise time to be determined by the capacity (CBUS) of bus line of R_{PU} and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

(2) The bus electric potential A to be determined by RPU and Rs at the moment when EEPROM outputs "L" to SDA bus should sufficiently secure the input "L" level (V_{IL}) of microcontroller including recommended noise margin $0.1V_{CC}$.

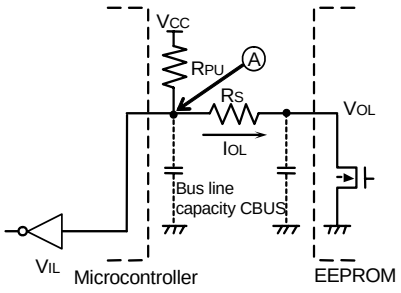


Figure 47. I/O circuit diagram

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leq V_{IL}$$

$$\therefore \quad R_S \leq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Example) When V_{cc}=3V, V_{IL}=0.3V_{CC}, V_{OL}=0.4V, R_{PU}=20kΩ,

$$\text{From (2)} \quad R_S \leq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$$

$$\leq 1.67[k\Omega]$$

○Minimum value of Rs

The minimum value of Rs is determined by over current at bus collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to EEPROM 10mA or below.

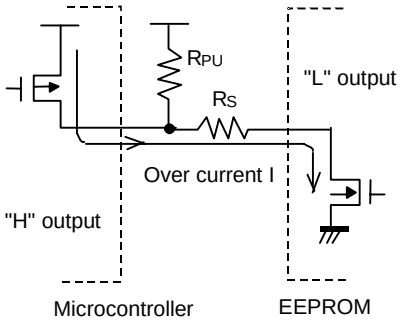


Figure 48. I/O Circuit diagram

$$\frac{V_{CC}}{R_S} \leqq I$$

$$\therefore \quad R_S \geqq \frac{V_{CC}}{I}$$

Example) When Vcc =3V, I = 10mA,

$$R_S \geqq \frac{3}{10\times10^{-3}}$$

$$\geqq 300[\Omega]$$

●**I²C BUS input / output circuit**

○Input (A2,SCL)

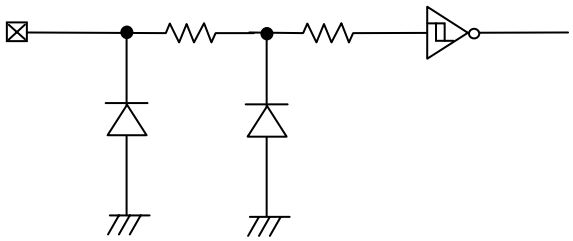


Figure 49. Input pin circuit diagram

○Input / output (SDA)

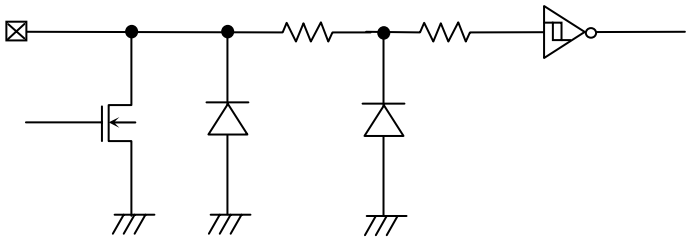


Figure 50. Input / output pin circuit diagram

○Input (WP)

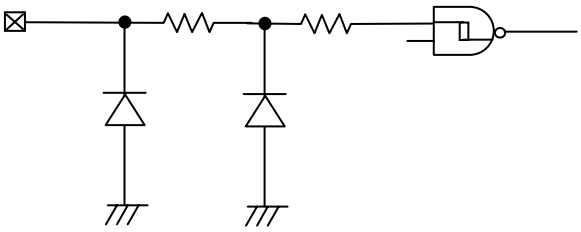


Figure 51. Input pin circuit diagram

●Notes on power ON

At power on, in IC internal circuit and set, Vcc rises through unstable low voltage area, and IC inside is not completely reset, and malfunction may occur. To prevent this, function of POR circuit and LVCC circuit are equipped. To assure the action, observe the following conditions at power on.

1. Set SDA= “H” and SCL = “L” or “H”.
2. Start power source so as to satisfy the recommended conditions of tR, tOFF, and Vbot for operating POR circuit.

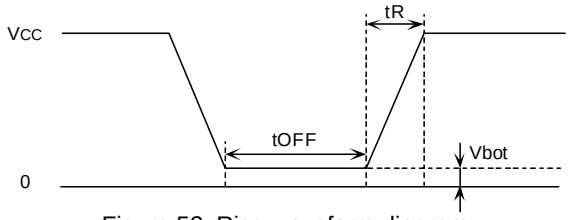


Figure 52. Rise waveform diagram

Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

3. Set SDA and SCL so as not to become “Hi-Z”.
   When the above conditions 1 and 2 cannot be observed, take the following countermeasures.
   a) In the case when the above condition 1 cannot be observed. When SDA becomes “L” at power on.
   → Control SCL and SDA as shown below, to make SCL and, “H” and “H”.

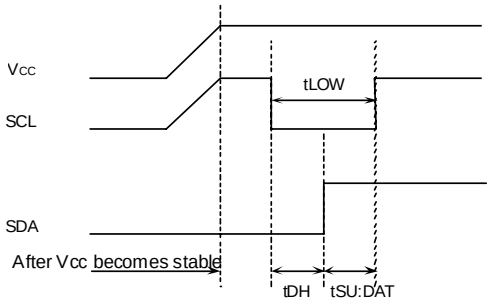


Figure 53. When SCL =”H” and SDA = “L”

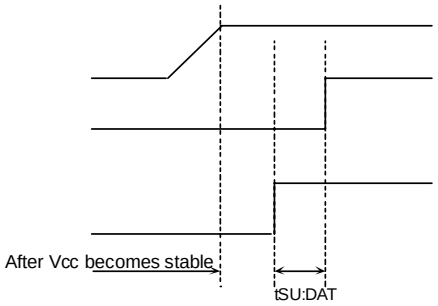


Figure 54. When SCL = “H” and SDA = “L”

   b) In the case when the above condition 2 cannot be observed.
   → After power source becomes stable, execute software reset (Page 16).

   c) In the case when the above conditions 1 and 2 cannot be observed.
   → Carry out a), and then carry out b).

●Low voltage malfunction prevention function

LVCC circuit prevents data rewrite action at low power, and prevents wrong write. At LVCC voltage (Typ. = 1.2V) or below, it prevent data rewrite.

●Vcc noise countermeasures

○Bypass capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC Vcc and GND. At that moment , attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

●Cautions on use

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(5) Thermal design
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal shortcircuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority.

●**Ordering Information**

B U 9 8 4 7 G U L - W	E 2

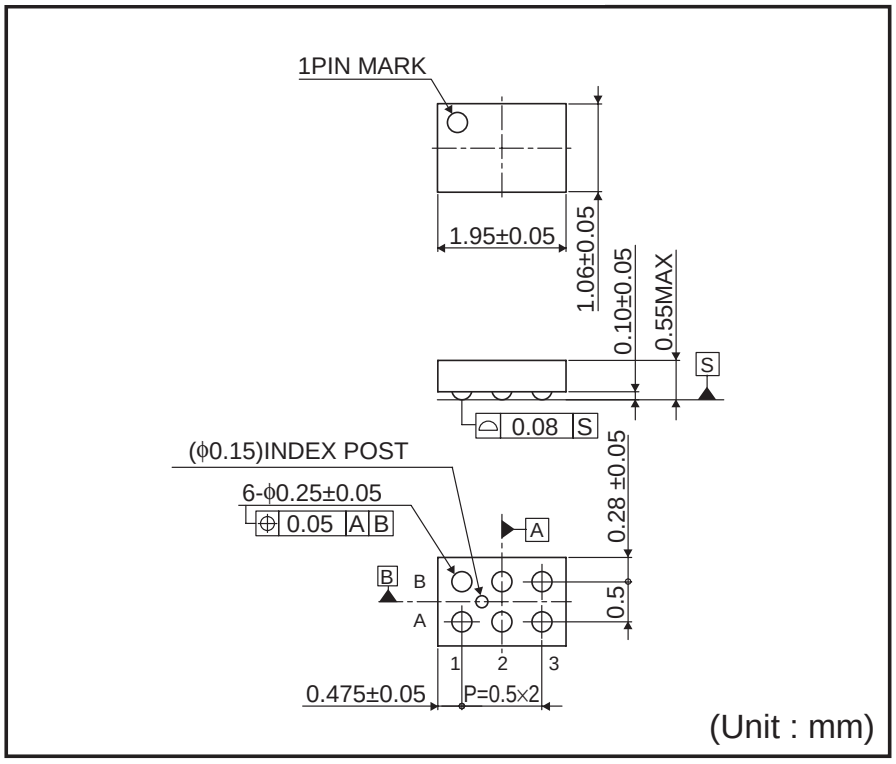
Part Number

Package
GUL : VCSP50L1 (BU9847GUL-W)

Packaging and forming specification
E2: Embossed tape and reel

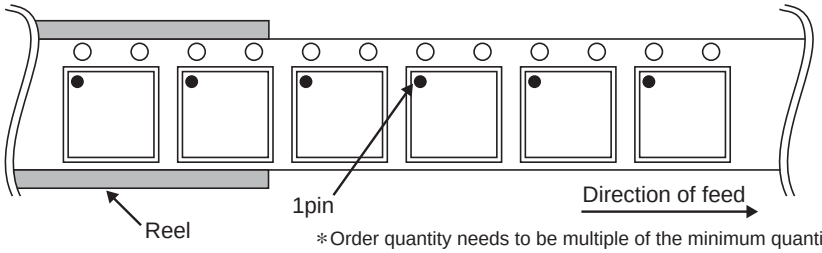
●**Physical Dimension Tape and Reel Information**

VCSP50L1 (BU9847GUL-W)



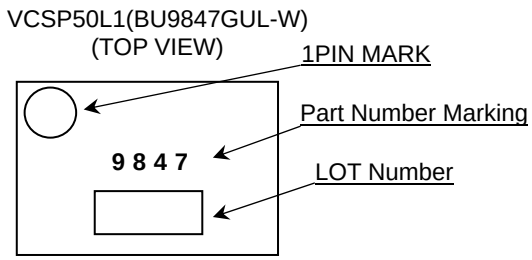
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



＊Order quantity needs to be multiple of the minimum quantity.

●**Marking Diagram**



●**Revision History**

Date	Revision	Changes
4.Sep.2012	001	New Release

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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