3.6V to 35V Input 1ch
Buck Controller
BD9845FV

General Description
BD9845FV is a switching regulator controller that uses pulse width modulation. This IC can be used for step-down DC/DC converter applications. BD9845FV is available in a compact package that is optimum for compact power supplies of many kinds of equipment.

Features
- Operates up to ($V_{CC}=35V$)
- Contains FET Driver Circuit (Step-Down Circuit 1 output).
- REG Output Circuit (2.5V) are contained.
- Built-In Over Current Protect
- Adjustable Soft Start and Pause Period.
- Three modes of Standby, Master, and Slave can be Switched. ($I_{CCS}=0 \mu A$ typ during standby)
- ON/OFF control is enabled independently for each channel. (DT terminal)

Applications
LCD, PDP, PC, AV, Printer, DVD, Projector TV, Fax, Copy Machine, Measuring Instrument, etc

Key Specifications
- Supply Voltage Range: 3.6V to 35V
- Error Amplifier Reference Voltage: 1.0V±1%
- Oscillation Frequency: 100kHz to 1500kHz
- Standby Current: 0µA(Typ)
- Operating Temperature Range: -40°C to +85°C

Package
W(Typ) x D(Typ) x H(Max)

Typical Application Circuit

Figure 1. Typical Application Circuit
**Pin Configuration**

(TOP VIEW)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VREF</td>
<td>Reference voltage (2.5V) output terminal</td>
</tr>
<tr>
<td>2</td>
<td>CT</td>
<td>Timing capacity external terminal</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>4</td>
<td>STB</td>
<td>Standby mode setting terminal</td>
</tr>
<tr>
<td>5</td>
<td>C5V</td>
<td>Output L side voltage (VCC-5V)</td>
</tr>
<tr>
<td>6</td>
<td>OUT</td>
<td>Output</td>
</tr>
<tr>
<td>7</td>
<td>VCC</td>
<td>Power terminal</td>
</tr>
<tr>
<td>8</td>
<td>OCP+</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>OCP-</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>SEL</td>
<td>Master/Slave mode setting terminal</td>
</tr>
<tr>
<td>11</td>
<td>FB</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>INV</td>
<td>Output error amplifier output terminal</td>
</tr>
<tr>
<td>13</td>
<td>SS</td>
<td>Output soft start time setting terminal</td>
</tr>
<tr>
<td>14</td>
<td>DT</td>
<td>Output dead time setting terminal</td>
</tr>
</tbody>
</table>

**Pin Description**

<table>
<thead>
<tr>
<th>Pin Number</th>
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<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VREF</td>
<td>Reference voltage (2.5V) output terminal</td>
<td>8</td>
<td>OCP+</td>
<td>Output over-current detector + input terminal</td>
</tr>
<tr>
<td>2</td>
<td>CT</td>
<td>Timing capacity external terminal</td>
<td>9</td>
<td>OCP-</td>
<td>Output over-current detector - input terminal</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground</td>
<td>10</td>
<td>SEL</td>
<td>Master/Slave mode setting terminal</td>
</tr>
<tr>
<td>4</td>
<td>STB</td>
<td>Standby mode setting terminal</td>
<td>11</td>
<td>FB</td>
<td>Output error amplifier output terminal</td>
</tr>
<tr>
<td>5</td>
<td>C5V</td>
<td>Output L side voltage (VCC-5V)</td>
<td>12</td>
<td>INV</td>
<td>Output error amplifier - input terminal</td>
</tr>
<tr>
<td>6</td>
<td>OUT</td>
<td>Output</td>
<td>13</td>
<td>SS</td>
<td>Output soft start time setting terminal</td>
</tr>
<tr>
<td>7</td>
<td>VCC</td>
<td>Power terminal</td>
<td>14</td>
<td>DT</td>
<td>Output dead time setting terminal</td>
</tr>
</tbody>
</table>

**Block Diagram**
### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>$V_{CC}$</td>
<td>36</td>
<td>V</td>
</tr>
<tr>
<td>Permissible Loss</td>
<td>$P_d$</td>
<td>0.50 (Note 1)</td>
<td>W</td>
</tr>
<tr>
<td>OUT Terminal Voltage</td>
<td>$V_{OUT}$</td>
<td>$V_{CC}-7V$ to $V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>C5V Terminal Voltage</td>
<td>$V_{C5V}$</td>
<td>$V_{CC}-7V$ to $V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>OCP Terminal Voltage</td>
<td>$V_{OCP}$</td>
<td>$V_{CC}-7V$ to $V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>Operation Temperature Range</td>
<td>$T_{opr}$</td>
<td>-40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{stg}$</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Joint Temperature</td>
<td>$T_{j,max}$</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(Note 1) When mounted on a 70.0 mm x 70.0 mm x 1.6 mm glass epoxy board. Derate by 4.0 mW/°C above $T_a=25$°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.

### Recommended Operating Conditions (Ta=25°C)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Range</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>$V_{CC}$</td>
<td>3.6 to 35</td>
<td>V</td>
</tr>
<tr>
<td>Output Terminal Voltage</td>
<td>$V_{OUT}$</td>
<td>$V_{C5V}$ to $V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>Timing Capacity</td>
<td>$C_{CT}$</td>
<td>47 to 3000</td>
<td>pF</td>
</tr>
<tr>
<td>Error Amplifier Input Voltage</td>
<td>$V_{INV}$</td>
<td>0 to $V_{REF}$-0.9</td>
<td>V</td>
</tr>
<tr>
<td>DT Terminal Input Voltage</td>
<td>$V_{DT}$</td>
<td>0 to $V_{REF}$</td>
<td>V</td>
</tr>
<tr>
<td>OCP+/− Input Voltage</td>
<td>$V_{OCP}$</td>
<td>$V_{CC}$±0.2</td>
<td>V</td>
</tr>
<tr>
<td>Oscillation Frequency</td>
<td>$f_{OSC}$</td>
<td>100 to 1500</td>
<td>kHz</td>
</tr>
<tr>
<td>STB Input Voltage</td>
<td>$V_{STB}$</td>
<td>0 to $V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>SEL Input Voltage</td>
<td>$V_{SEL}$</td>
<td>0 to $V_{CC}$</td>
<td>V</td>
</tr>
</tbody>
</table>
### Electrical Characteristics

(Unless otherwise specified, Ta=25°C, V<sub>CC</sub>=6V)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Standard Value</th>
<th>Conditions</th>
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</thead>
<tbody>
<tr>
<td><strong>[VREF Output Unit]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td>V&lt;sub&gt;REF&lt;/sub&gt;</td>
<td>2.450</td>
<td>2.500</td>
</tr>
<tr>
<td>Input Stability(Line Reg.)</td>
<td>V&lt;sub&gt;L'&lt;/sub&gt;&lt;sub&gt;REG&lt;/sub&gt;</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Load Stability(Reg.)</td>
<td>V&lt;sub&gt;LO'&lt;/sub&gt;&lt;sub&gt;REG&lt;/sub&gt;</td>
<td>-</td>
<td>2</td>
</tr>
<tr>
<td>Current Capacity</td>
<td>I&lt;sub&gt;MAX&lt;/sub&gt;</td>
<td>2</td>
<td>13</td>
</tr>
<tr>
<td><strong>[Triangular Wave Oscillator]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Oscillation Frequency</td>
<td>f&lt;sub&gt;OSC&lt;/sub&gt;</td>
<td>95</td>
<td>106</td>
</tr>
<tr>
<td>Frequency Fluctuation</td>
<td>f&lt;sub&gt;FL&lt;/sub&gt;</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td><strong>[Soft Start Unit]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SS Source Current</td>
<td>I&lt;sub&gt;SSSO&lt;/sub&gt;</td>
<td>1.4</td>
<td>2</td>
</tr>
<tr>
<td>SS Sink Current</td>
<td>I&lt;sub&gt;SSSI&lt;/sub&gt;</td>
<td>5</td>
<td>12</td>
</tr>
<tr>
<td><strong>[Pause Period Adjusting Circuit]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DT Input Bias Current</td>
<td>I&lt;sub&gt;IDT&lt;/sub&gt;</td>
<td>-</td>
<td>0.1</td>
</tr>
<tr>
<td>DT Sink Current</td>
<td>I&lt;sub&gt;IDTSI&lt;/sub&gt;</td>
<td>1</td>
<td>3.3</td>
</tr>
<tr>
<td><strong>[Low Input Malfunction Preventing Circuit]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Threshold Voltage</td>
<td>V&lt;sub&gt;UTH&lt;/sub&gt;</td>
<td>3.0</td>
<td>3.2</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>V&lt;sub&gt;UHYS&lt;/sub&gt;</td>
<td>-</td>
<td>0.15</td>
</tr>
<tr>
<td><strong>[Error Amplifier]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Non-Inverting Input Reference Voltage</td>
<td>V&lt;sub&gt;INV&lt;/sub&gt;</td>
<td>0.99</td>
<td>1</td>
</tr>
<tr>
<td>Reference Voltage Supply Fluctuation</td>
<td>dV&lt;sub&gt;INV&lt;/sub&gt;</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>INV Input Bias Current</td>
<td>I&lt;sub&gt;II&lt;/sub&gt;</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>Open Gain</td>
<td>AV</td>
<td>65</td>
<td>85</td>
</tr>
<tr>
<td>Max Output Voltage</td>
<td>V&lt;sub&gt;FBH&lt;/sub&gt;</td>
<td>2.30</td>
<td>-</td>
</tr>
<tr>
<td>Min Output Voltage</td>
<td>V&lt;sub&gt;FBL&lt;/sub&gt;</td>
<td>-</td>
<td>0.6</td>
</tr>
<tr>
<td>Output Sink Current</td>
<td>I&lt;sub&gt;FR&lt;/sub&gt;</td>
<td>0.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Output Source Current</td>
<td>I&lt;sub&gt;FSO&lt;/sub&gt;</td>
<td>50</td>
<td>105</td>
</tr>
<tr>
<td><strong>[PWM Comparator]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Threshold Voltage (f&lt;sub&gt;OSC&lt;/sub&gt;=100kHz)</td>
<td>V&lt;sub&gt;THD&lt;/sub&gt;</td>
<td>1.4</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;THD&lt;/sub&gt;</td>
<td>1.9</td>
<td>2</td>
</tr>
<tr>
<td><strong>[Output Unit]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output ON Resistance H</td>
<td>R&lt;sub&gt;RN&lt;/sub&gt;</td>
<td>-</td>
<td>4.0</td>
</tr>
<tr>
<td>Output ON Resistance L</td>
<td>R&lt;sub&gt;ON&lt;/sub&gt;</td>
<td>-</td>
<td>3.3</td>
</tr>
<tr>
<td>CSV Clamp Voltage</td>
<td>V&lt;sub&gt;CLMP&lt;/sub&gt;</td>
<td>4.5</td>
<td>5</td>
</tr>
<tr>
<td><strong>[Over-Current Protection Circuit]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Over-Current Detection Threshold Voltage</td>
<td>V&lt;sub&gt;DC&lt;/sub&gt;&lt;sub&gt;TH&lt;/sub&gt;</td>
<td>0.04</td>
<td>0.05</td>
</tr>
<tr>
<td>OCP-Input Bias Current</td>
<td>I&lt;sub&gt;OCP&lt;/sub&gt;</td>
<td>-</td>
<td>0.1</td>
</tr>
<tr>
<td>Over-Current Detection Delay Time</td>
<td>t&lt;sub&gt;OCP&lt;/sub&gt;</td>
<td>-</td>
<td>200</td>
</tr>
<tr>
<td>Over-Current Detection Minimum Retention Time</td>
<td>t&lt;sub&gt;OCP&lt;/sub&gt;</td>
<td></td>
<td>0.8</td>
</tr>
<tr>
<td><strong>[Standby Changeover Unit]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>STB Flow-In Current</td>
<td>I&lt;sub&gt;STB&lt;/sub&gt;</td>
<td>-</td>
<td>55</td>
</tr>
<tr>
<td>Standby Mode Setting Range</td>
<td>V&lt;sub&gt;STSH&lt;/sub&gt;</td>
<td>3.0</td>
<td>-</td>
</tr>
<tr>
<td>Active (Master) Mode Setting Range</td>
<td>V&lt;sub&gt;SELH&lt;/sub&gt;</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>SEL Flow-In Current</td>
<td>I&lt;sub&gt;SEL&lt;/sub&gt;</td>
<td>-</td>
<td>15</td>
</tr>
<tr>
<td>Master Mode Setting Range</td>
<td>V&lt;sub&gt;SELH&lt;/sub&gt;</td>
<td>2.0</td>
<td>-</td>
</tr>
<tr>
<td>Slave Mode Setting Range</td>
<td>V&lt;sub&gt;SELH&lt;/sub&gt;</td>
<td>2.0</td>
<td>-</td>
</tr>
<tr>
<td><strong>[Device Overall]</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standby Current</td>
<td>I&lt;sub&gt;CCS&lt;/sub&gt;</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>Average Power Consumption</td>
<td>I&lt;sub&gt;CCA&lt;/sub&gt;</td>
<td>1</td>
<td>2.4</td>
</tr>
</tbody>
</table>
Typical Performance Curves

Figure 2. Standby Current vs Ambient Temperature

Figure 3. Circuit Current vs Supply Voltage

Figure 4. Circuit Current vs Ambient Temperature

Figure 5. Reference Voltage vs Supply Voltage
Typical Performance Curves – continued

Figure 6. Reference Voltage vs Reference Output Current (VREF Current Capability)

Figure 7. Reference Output Voltage vs Ambient Temperature (VREF Temperature Characteristics)

Figure 8. UVLO Threshold vs Ambient Temperature

Figure 9. Loop Gain vs Frequency (Error Amplifier I/O Characteristics)
Typical Performance Curves – continued

Figure 10. Error Amplifier Input Current vs Error Amplifier Input Voltage

Figure 11. Error Amplifier Reference Voltage vs Ambient Temperature

Figure 12. FB Source Current vs Error Amplifier Output Voltage

Figure 13. FB Sink Current vs Error Amplifier Output Voltage
Typical Performance Curves – continued

**Figure 14. Soft Start Source Current vs Soft Start Voltage**

**Figure 15. Soft Start Sink Current vs Soft Start Voltage**

**Figure 16. Soft Start Source Current vs Ambient Temperature**

**Figure 17. Oscillation Frequency vs Ambient Temperature**
Typical Performance Curves – continued

Figure 18. DT Input Bias Current vs DT Input Voltage

Figure 19. DT Sink Current vs DT Input Voltage

Figure 20. Output Duty Cycle vs DT Input Voltage (100kHz)

Figure 21. Output Duty Cycle vs DT Input Voltage (1.5MHz)
Typical Performance Curves - continued

Figure 22. $I_{DS}$ vs Output Voltage (Output ON Resistance H ($R_{ONH}$))

Figure 23. $I_{DS}$ vs Output Voltage (Output ON Resistance L ($R_{ONL}$))

Figure 24. STB Flow-In Current vs STB Input Voltage

Figure 25. Over-Current Detection Threshold Voltage vs Ambient Temperature
Typical Performance Curves - continued

Figure 26. C5V Saturation Voltage

Figure 27. C5V Load Regulation

Figure 28. C5V Line Regulation
Application Information

1. Operation Description of Each Block and Function
   (1) REG: Reference Voltage Unit
   The REG (2.5V) produces a voltage of 2.5V which is more stable than the supply voltage input to VCC terminal. This voltage is used as a reference voltage to the IC’s internal circuitry. This voltage is also connected to the VREF terminal. Insert a capacitor of 0.1µF to VREF terminal.
   The REG (Vcc-5V) produces a voltage of (Vcc-5V) which is used as power supply (LDO) of driver circuit (DRV). This voltage is also connected to the C5V terminal. Insert a capacitor of 1µF between VCC and C5V terminals.

   (2) ERR Amp: Error Amplifier
   In step-down application, the inverting input, INV, of the error amplifier detects output voltage by sending back feedback current from final output stage (on load side) of switching regulator. Resistors R1 and R2 that are connected to this input terminal are used for setting the output voltage. The non-inverting input of the amplifier is connected to an internal reference voltage (1.0V). R1 and CF, which are connected between FB, the output of the error amplifier, and INV, are for setting of the amplifier’s loop gain.
   FB is connected to the non-inverting input of PWM Comp.
   Setting of output voltage (VOUT) is as follows:
   \[ V_{OUT} = \frac{R2}{R1 + R2} \times 1.0V \]

   (3) OSC: Triangular Wave Oscillating Unit
   This generates a triangular wave which is input to the PWM Comp.
   First, timing capacitor, C_CT, which is connected between CT terminal and GND, is charged by a constant current of 200 µA which is generated inside the IC. When CT voltage reaches 2.0 V typ, the comparator is switched, and then C_CT is discharged by a constant current of 200 µA. Then, when CT voltage reaches 1.5V, the comparator is switched again, and C_CT is charged again. This repetition generates the triangular wave.

   Oscillation frequency is determined by the externally mounted C_CT through the formula below:
   \[ f_{osc} \approx \frac{IC}{(2 \cdot C CT \cdot \Delta V_{osc})} \]
   where:
   IC is the CT sink/source current 200 µA typ
   \( \Delta V_{osc} \) is the triangular wave amplifying voltage = (VT0 - V100) = 0.50V Typ

   The error from the formula is caused by the delay introduced to the internal circuit when operated at a high frequency. See the graph in Figure 30 for the setting.
   This triangular wave can be probed through CT terminal. It is also possible to use an external oscillator by switching to slave mode which is described later. Waveform input here in principle must be a triangular wave of Vpeak = (1.5V ↔ 2.0V) which is equivalent to internal oscillation circuit.

   External input voltage range
   \[ VCT : \quad 1.4V < VCT < 2.3V \]

   Standard external C_CT range
   \[ C_CT : \quad (\text{Min}) 47 \text{pF} - (\text{Max}) 3000 \text{pF} \]
(4) Soft Start : Soft Start Function
It is possible to provide SS terminal (pin 13) with soft start function by connecting C_{SS} as shown in figure 31.
Soft start time \( t_{SS} \) is shown by the formula below:

\[
I_{SS} = C_{SS} \cdot \frac{V_{IN}}{I_{SSO}}
\]

where:
- \( C_{SS} \) is the SS terminal connection capacitance
- \( V_{IN} \) is the Error amplifier reference voltage (1V typ)
- \( I_{SSO} \) is the SS source current (2\( \mu \)A typ)

(Ex) When \( C_{SS} = 0.01 \) \( \mu \)F

\[
t_{SS} = \frac{0.01 \times 10^{-6} \times 1}{2 \times 10^{-6}} = 5 \text{[msec]}
\]

In order for soft start to function, soft start time must be set longer than the start time of power supply and STB.
It is also possible to provide soft start by connecting the resistors (\( R_1, R_2 \)) and capacitor (\( C_{DT} \)) to DT terminal (14pin) as shown in figure 32.

(5) PWM Comp - DEAD TIME: Pause Period Adjusting Circuit - Dead Time
Dead time can be set by applying voltage dividing resistors between VREF and GND to DT terminal.
PWM Comp compares the input dead time voltage (DT terminal voltage) and error voltage from Err Amp (FB terminal voltage) with triangular wave, and turns the output off and on. When dead time voltage < error voltage, duty of output is determined by dead time voltage. (When dead time setting is not used, pull up DT terminal to VREF terminal with resistor approx 10 k ohms.)
Dead time voltage \( V_{DT} \) in Figure 31 is shown by the formula below:

\[
V_{DT} = V_{REF} \cdot \frac{R_2}{R_1 + R_2}
\]

Relation between \( V_{DT} \) and Duty [See the graph on the right.]

<table>
<thead>
<tr>
<th>Duty % 100%</th>
<th>Duty 0%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>When ( f ) = 100kHz</td>
<td>1.9</td>
</tr>
<tr>
<td>When ( f ) = 1.5MHz</td>
<td>1.95</td>
</tr>
</tbody>
</table>

[Unit : V]

Be careful when oscillation frequency is high, the upper/lower amplitude limit of the triangular wave (\( V_{IN(100V/V_0)} \)) increases due to the shift in the delay time of the comparator.

(6) OCP Comp: Over-current Detection Circuit
This function provides protection by forcibly turning off the output when abnormal over-current flows due to shorting of output, etc. When the voltage across the sense resistor, which is between the terminals OCP+(8pin) and OCP-(9pin), exceeds the over-current detection voltage of 50 mV (typ), which is determined as over-current condition, the switching operation is stopped immediately by setting OUT to HIGH and DT, SS and FB to LOW.
Switching operation is automatically restored when the voltage between the terminals OCP+ and OCP- is below over-current detection voltage.
In addition, although hysteresis, etc. are not set here, the minimum detection retention time of 1.6 ms (typ) is set to suppress the heating of FET, etc. (See the timing chart.)
To disable over-current detection, short both OCP+ and OCP- terminals to VCC pin.
(7) STB /SEL: Standby/Master/Slave Function
Standby mode and normal mode can be switched by STB terminal (4pin).
(a) When STB<0.5V, standby mode is set.
Output stops (OUT=HIGH), REG stops and there is no circuit current (Isc = 0 µA).
(b) When STB>3.0V, normal operation mode is set.
All circuits operate. Use the controller normally in this range.

Master mode and slave mode can be switched by SEL terminal (10pin).
(a) When SEL<0.5V, master mode is set.
All circuits operate.
(b) When SEL>2.0V, slave mode is set.
Operation status is set, but OSC block is stopped, CT terminal is High-Z here, and triangular wave is not outputted (PWM circuit and protection circuit perform the same operation as usual.). Therefore, if the controller is used in this mode, triangular wave is not outputted, operation is unstable, and normal output cannot be obtained. Be careful when using the IC in this mode.

(8) OUT (Output: External FET Gate Drive)
OUT terminal (6pin) is capable of directly driving the gate of external (PchMOS) FET. Amplitude of output is restricted between VCC and C5V (Vcc-5V), and is not restricted by input voltage to gate, which allows broad selection of FET.
However, for precaution when selecting FET, there is a restriction that input capacitance of gate is determined by current capability of C5V and permissible loss of IC. Refer to the permissible range on the graph in figure 35 when determining FET.

(9) Protection: Other Protection Functions
This IC is equipped with low input malfunction prevention circuit (UVLO) and abnormal temperature protection circuit (TSD) besides over-current detection circuit (OCP).
Low input malfunction prevention circuit is for preventing unstable output when input voltage is low.
Three voltages are monitored: VCC (3.2V), VREF(2.35V), and C5V(Vcc-3V), and they have output only when the UVLO for the three voltages are canceled. (See the timing chart.)
Abnormal temperature protection circuit is for protecting the IC from destruction by preventing thermal runaway when the IC is operating above the rated temperature. (It does not operate normally.)
Apply a design with allowable margin for heating in consideration of permissible loss.
2. Timing Chart

**Starting characteristics (UVLO cancel) and standby operation**

![Timing Chart](image)

**UVLO Voltage [unit: V]**

<table>
<thead>
<tr>
<th>Item</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold Voltage (VCC)</td>
<td>3.0</td>
<td>3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>-</td>
<td>0.15</td>
<td>0.25</td>
</tr>
<tr>
<td>Threshold Voltage (VREF)</td>
<td>2.0</td>
<td>2.2</td>
<td>2.4</td>
</tr>
<tr>
<td>Threshold Voltage (CSV)</td>
<td>-</td>
<td>3.0</td>
<td>3.4</td>
</tr>
</tbody>
</table>

**Over-current detection (When output is shorted: Over-current detection and cancel are repeated at a specified time interval.)**

![Over-current Detection](image)
3. Example of Application Circuit

Figure 36

(1) Setting of Output Unit Coil (L) and Capacitor (C₀)
In a step-down application, set the coil and capacitor as follows:

<Setting of L-Value>
When load current gets high, the current flowing through the coil gets continuous, and the relation below is established:

\[ L = \frac{t_{SW}}{\Delta I_L} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \]

where:
\( V_{IN} \) is the input voltage
\( t_{SW} \) is 1/(switching frequency)
\( \Delta I_L \) is ripple current of coil

Normally set \( \Delta I_L \) below 30% of the maximum output current (\( I_{OMAX} \)).
When L-value is increased, the ripple current (\( \Delta I_L \)) decreases. In general, the greater the L-value, the smaller the permissible current of coil gets, and when the current exceeds permissible current, the coil is saturated and L-value changes. Contact the coil manufacturer and check permissible current.

<Setting of Output Capacitor C₀>
Select an output capacitor C₀ by ESR (equivalent series resistance) property of capacitor.
Output ripple voltage (Delta V₀) is almost the ESR of the output capacitor, therefore,

\[ \Delta V_{OUT} \approx \Delta I_L \times ESR \]

where:
ESR is the equivalent series resistance of output capacitor C₀

The relation above is established.
Ripple component of output capacitor is small enough to be neglected in comparison with ripple component of ESR in many cases. As for C₀ value, it is recommended to use a sufficiently large capacitor with a capacitance that satisfies ESR condition.
<Switching Element>
Decide the switching element by using the peak current. Peak current $I_{SW \text{ peak}}$ flowing through the switching element is equal to the peak current flowing through the coil, therefore the equation below is established.

$$I_{SW \text{ peak}} = I_{OUT} + \Delta I_L / 2$$

Select a switching element of permissible current and having enough margin over the peak current calculated by the equation above.

For Noise reduction and efficiency improvement, select a FET having an input capacitance ($C_{iss}$ and $Q_g$), On resistance as small as possible, and a Schottky diode having an inter-terminal capacitance, reverse recovery time $t_{rr}$ and forward voltage $V_F$ as small as possible.

<Input capacitor $C_{IN}$>
The bypass capacitor of VCC is used by both electrolytic capacitor and ceramic capacitor. The ceramic capacitor is placed near each channel Pow-FET drain pin as possible because of supplied output switching current instantaneously from input capacitor ($C_{in}$).

In case of using an electrolytic capacitor, confirm permissible ripple current.

(2) Example of Over-current Protection Circuit
Insert a sense resistor between the source and VIN of output Pch-FET for detecting over-current as shown in Figure 37.

Refer to the formula below for determining the value of the sense resistor. Provide margin for permissible loss.

$$R_{SENSE} = \frac{V_{OCPTH}}{I_{OCP}}$$

where:
- $V_{OCPTH}$ is over-current detection voltage (50 mV typ)
- $I_{OCP}$ is over-current detection setting current

$I_{OCP}$ is a peak current $I_{SW \text{ peak}}$ here, and the amperage for output load is an over-current setting amperage minus ripple current component (Delta $I_L/2$), etc. (See the formula on P16.)

There is a time delay of approximately 200ns from detection until the output is stopped (pulse of approximately 100 ns causes delay time but detection is made), and an error may be caused from the value above. In addition, the input to over-current detection unit is very sensitive that wrong detection due to noise may be possible. When wrong detection occurs, try to eliminate noise by using resistors $R_1$ and $R_2$ or capacitors $C_1$, $C_2$, $C_3$, and $C_4$ shown in Figure 37.
To take measure to switching noise for OCP+/− input.
The input of over current protection (OCP) block is too sensitive to stop each ON pulse for protecting external components. The response time of OCP is about 100nsec (Max 200nsec), but OCP block can respond at 20nsec to 30nsec to bigger pulse.
Therefore, it is possible to miss-operate by switching noise. (See Figure 38)
To prevent miss-operation of OCP, a low pass filter should be insert in OCP+ and OCP− pins. (Refer Figure 37) When cut off frequency of the low pass filter decreases, OCP− voltage become blunt, and it prevents to miss-operates OCP detection from turning on switching noise. But, in over-decreasing, the detection current level is bigger. In most cases, it is set R2=100hm to 470hm, C5=1000pF to 2200pF, and cut off frequency is over 10 times of OSC frequency.
In case the effect of inserting low pass filter is not enough, the switching noise must decrease on application board to use below item.

- High current pattern must be shorted as possible on PCB.
- Bypass capacitor C4 is nearly and using high value.
- Using Gate resistor Rgate.

**Figure 38**

Other attention, the voltage between VCC and OCP+/OCP− pin must be under 0.2V. So the capacitor must be not connected between OCP+/− and GND pin. Common mode differential input range of OCP+/OCP− is provided from Vcc+0.7V to Vcc−2.5V.
(3) Example of Master/Slave (Sync Multi-Ch Output) Operation Circuit

This IC is set to slave mode by setting the input of STB terminal at 2.5V±0.1V, and multi-channel output is enabled with frequency synchronized. (Figure 39) However, CT terminal has a high impedance in slave mode, and triangular wave is generated by CT waveform of master mode IC. Therefore the example of master/slave circuit below is recommended to avoid malfunction by start/stop timing of master IC and slave IC. As for output, it is recommended to control ON/OFF reliably with DT terminal. 

An example of master/slave circuit configuration is shown below.

Also, oscillation frequency is determined by capacitor (C<sub>CT</sub>) connected to CT. When the slave ICs are large in number and oscillation frequency is high, parasitic capacitance due to board wiring in contact with CT cannot be ignored, and preset frequency may drift. Care must be considered.

An example of master/slave circuit configuration is shown below.

Figure 39

(4) About Board Layout

In order to make full use of the IC’s performance, fully understand the items below besides the general precautions.

(a) OCP+/OCP- outputs are sensitive. Please refer to (2)Example of Over-current Protection Circuit

(b) Try to make the wiring as short as possible to avoid noise and keep away from noise line (Especially OCP+/-, FB and CT are sensitive lines).

(c) Please put layout for dummy pattern of C, R around OCP and phase compensation circuit.

(d) Switching of large current is likely to generate noise. Try to make the large current route (VIN, Rsense, FET, L, Di, and Cout) as thick and short as possible, and try to apply one-point grounding for GND. OUT terminal is also a switching line, and it must be wired as short as possible. (When multi-layer board is used, shielding by intermediate layer also seems to be effective.)

(e) Please put Bypass capacitors nearby IC and FET/Di.

(f) C<sub>CT</sub> and C<sub>VREF</sub> are voltage references, so they must be wired with the shortest distance to GND to be protected against external influence.

(g) The VCC and GND nodes should both be wide to reduce line impedance and to keep the noise and voltage drop low. So be careful not to allow common impedance to GND lines of sensitive functions (Ex. Capacitor of CT and VREF).

When only one channel is used, connect unused channels as shown above.

Figure 41
### I/O Equivalent Circuit

<table>
<thead>
<tr>
<th>Pin Configuration</th>
<th>Symbolic Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>2pin (CT)</td>
<td><img src="image" alt="2pin Circuit" /></td>
</tr>
<tr>
<td>14pin (DT)</td>
<td><img src="image" alt="14pin Circuit" /></td>
</tr>
<tr>
<td>13pin (SS)</td>
<td><img src="image" alt="13pin Circuit" /></td>
</tr>
<tr>
<td>12pin (INV)</td>
<td><img src="image" alt="12pin Circuit" /></td>
</tr>
<tr>
<td>11pin (FB)</td>
<td><img src="image" alt="11pin Circuit" /></td>
</tr>
<tr>
<td>9pin (OCP-)</td>
<td><img src="image" alt="9pin Circuit" /></td>
</tr>
<tr>
<td>5pin (C5V)</td>
<td><img src="image" alt="5pin Circuit" /></td>
</tr>
<tr>
<td>6pin (OUT)</td>
<td><img src="image" alt="6pin Circuit" /></td>
</tr>
<tr>
<td>8pin (OCP+)</td>
<td><img src="image" alt="8pin Circuit" /></td>
</tr>
<tr>
<td>4pin (STB)</td>
<td><img src="image" alt="4pin Circuit" /></td>
</tr>
<tr>
<td>10pin (SEL)</td>
<td><img src="image" alt="10pin Circuit" /></td>
</tr>
<tr>
<td>1pin (VREF)</td>
<td><img src="image" alt="1pin Circuit" /></td>
</tr>
<tr>
<td>3pin (GND), 7pin (VCC)</td>
<td><img src="image" alt="3pin Circuit" /></td>
</tr>
</tbody>
</table>

**Legend:**
- **CT:** Common Terminal
- **DT:** Digital Terminal
- **SS:** Signal Source
- **INV:** Inverter
- **VCC:** Power Supply
- **VREF:** Reference Voltage
- **C5V:** 5V Supply
- **OUT:** Output
- **OCP-:** Overcurrent Protection
- **OCP+:** Overcurrent Protection
- **SEL:** Selection
- **STB:** Status
- **GND:** Ground
Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC’s power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC’s power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.
Operational Notes – continued

11. Unused Input Pins
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

Figure 42. Example of monolithic IC structure
Ordering Information

<table>
<thead>
<tr>
<th>B</th>
<th>D</th>
<th>9</th>
<th>8</th>
<th>4</th>
<th>5</th>
<th>F</th>
<th>V</th>
<th>E</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part Number</td>
<td>Package</td>
<td>FV: SSOP-B14</td>
<td>Packaging and forming specification</td>
<td>E2: Embossed tape and reel</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Marking Diagram

SSOP-B14 (TOP VIEW)

- Part Number Marking
- LOT Number
- 1PIN MARK
Physical Dimension, Tape and Reel information

<table>
<thead>
<tr>
<th>Package Name</th>
<th>SSOP-B14</th>
</tr>
</thead>
</table>

**Physical Dimensions**

- Width: 5.0 ± 0.2 mm
- Length: 8.4 ± 0.3 mm
- Tape: 0.65 mm
- Reel: 0.15 ± 0.1 mm

**Tape and Reel Information**

- **Type:** Embossed carrier tape
- **Quantity:** 2500 pcs
- **Direction of feed:**
  - The direction is the 1st position at the upper left when you hold the reel on the left hand and pull out the tape on the right hand.

**Notes:**
- Order quantity needs to be a multiple of the minimum quantity.
## Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>06.Nov.2015</td>
<td>001</td>
<td>New Release</td>
</tr>
</tbody>
</table>
Notice

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(Note1) Medical Equipment Classification of the Specific Applications

<table>
<thead>
<tr>
<th>JAPAN</th>
<th>USA</th>
<th>EU</th>
<th>CHINA</th>
</tr>
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<tr>
<td>CLASS III</td>
<td>CLASS III</td>
<td>CLASS II b</td>
<td>CLASS III</td>
</tr>
<tr>
<td>CLASS IV</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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[c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
[d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
[e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
[f] Sealing or coating our Products with resin or other coating materials
[g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
[h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

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