Power Supply IC Series for TFT-LCD Panels

12V Input Multi-channel System Power Supply IC

BD8160AEFV

● Description
The BD8160AEFV is a system power supply for the TFT-LCD panels used for liquid crystal TVs. It incorporates two high-power FETs with low on resistance for large currents that employ high-power packages, thus driving large current loads while suppressing the generation of heat. A charge pump controller is incorporated as well, thus greatly reducing the number of application components.

● Features
1) Step-up and step-down DC/DC converter
2) Incorporates 2.6 A N-channel FET.
3) Incorporates positive/negative charge pumps.
4) Input voltage limit: 8 V to 18 V
5) Feedback voltage: 1.162 V ± 1%
6) Switching frequency: 500 kHz / 750kHz
7) Protection circuit: Under voltage lockout protection circuit
   Thermal shutdown circuit
   Overcurrent protection circuit
   Short Circuit Protection
   Overvoltage protection circuit for VS voltage (Boost DC/DC output)
8) HTSSOP-B28 Package

● Applications
Power supply for the TFT-LCD panels used for LCD TVs

● Absolute maximum ratings (Ta = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>SUP,VIN</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Pd</td>
<td>4700*</td>
<td>mW</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>Topr</td>
<td>-40~+85</td>
<td>℃</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>Tstg</td>
<td>-55~+150</td>
<td>℃</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>Tjmax</td>
<td>150</td>
<td>℃</td>
</tr>
<tr>
<td>SW Voltage</td>
<td>Vsw</td>
<td>21</td>
<td>V</td>
</tr>
<tr>
<td>SWB Voltage</td>
<td>Vswb</td>
<td>19</td>
<td>V</td>
</tr>
<tr>
<td>EN1,EN2 Voltage</td>
<td>VEN1,VEN2</td>
<td>19</td>
<td>V</td>
</tr>
</tbody>
</table>

* Derating in done 37.6mW/℃ for operating above Ta ≥ 25℃(On 4-layer 70.0mm × 70.0mm × 1.6mm board)

● Recommendable Operation Range (Ta=25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>SUP,VIN</td>
<td>8</td>
<td>12</td>
</tr>
<tr>
<td>Vs Voltage</td>
<td>Vsw</td>
<td>VIN+2</td>
<td>15</td>
</tr>
<tr>
<td>Switch current for SW</td>
<td>Isw</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Switch current for SWB</td>
<td>Isw</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>EN1,EN2,FREQ Voltage</td>
<td>VEN1,VEN2,VFREQ</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

** Pd, ASO should not be exceeded
### Electrical characteristics (unless otherwise specified VIN=12V and Ta=25°C)

#### 1. DC/DC converter controller block

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limits</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soft start – SS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SS source current</td>
<td>I_{SS}</td>
<td>6</td>
<td>10</td>
<td>14 µA, V_{SS}=0.5V</td>
</tr>
<tr>
<td>Error amplifier block – FB and FBB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB and FBB input bias current</td>
<td>I_{FB,12}</td>
<td>-</td>
<td>0.1</td>
<td>2 µA</td>
</tr>
<tr>
<td>Feedback voltage for boost converter</td>
<td>V_{FB}</td>
<td>1.150</td>
<td>1.162</td>
<td>1.174 V, Voltage follower</td>
</tr>
<tr>
<td>Feedback voltage for buck converter</td>
<td>V_{FBB}</td>
<td>1.188</td>
<td>1.213</td>
<td>1.238 V</td>
</tr>
<tr>
<td>SW block – SW</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On resistance N-channel</td>
<td>R_{ONN}</td>
<td>-</td>
<td>0.2</td>
<td>0.3 Ω, I_{O}=0.8A</td>
</tr>
<tr>
<td>Leak current N-channel</td>
<td>I_{LEAKN1}</td>
<td>-</td>
<td>0</td>
<td>10 µA, V_{SW}=18V</td>
</tr>
<tr>
<td>Switch current limit for SW</td>
<td>I_{SW}</td>
<td>-</td>
<td>-</td>
<td>- A</td>
</tr>
<tr>
<td>Maximum duty cycle</td>
<td>M_{DUTY}</td>
<td>75</td>
<td>90</td>
<td>97 %, FB= 0V</td>
</tr>
<tr>
<td>SW block – SWB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On resistance N-channel</td>
<td>R_{ONH}</td>
<td>-</td>
<td>0.2</td>
<td>0.3 Ω, I_{O}=0.8A</td>
</tr>
<tr>
<td>Leak current N-channel</td>
<td>I_{LEAKN2}</td>
<td>-</td>
<td>0</td>
<td>10 µA, V_{NB}=18V, V_{SWB}=0V</td>
</tr>
<tr>
<td>Switch current limit for SWB</td>
<td>I_{SWB}</td>
<td>2.0</td>
<td>-</td>
<td>- A</td>
</tr>
<tr>
<td>Protections</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Over Voltage Protection for SW</td>
<td>V_{SWOVP}</td>
<td>18.5</td>
<td>19</td>
<td>19.5 V</td>
</tr>
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</table>

#### 2. Charge pump driver block

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limits</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Error amplifier block – FBP and FBN</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FBP, FBN input bias current</td>
<td>I_{FB,1, FBN}</td>
<td>-</td>
<td>0.1</td>
<td>1 µA</td>
</tr>
<tr>
<td>Feedback voltage for VGH</td>
<td>V_{FB}</td>
<td>1.188</td>
<td>1.213</td>
<td>1.238 V</td>
</tr>
<tr>
<td>Feedback voltage for VGL</td>
<td>V_{FBN}</td>
<td>0.18</td>
<td>0.2</td>
<td>0.22 V</td>
</tr>
<tr>
<td>Delay start block</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DLY1, DLY2 source current</td>
<td>I_{DLY1, DLY2}</td>
<td>2</td>
<td>5</td>
<td>9 µA, V_{DLV}=0.5V</td>
</tr>
<tr>
<td>DRP, DRN block</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On resistance N-channel</td>
<td>R_{ONN}</td>
<td>-</td>
<td>5</td>
<td>- Ω, I_{O}=20mA</td>
</tr>
<tr>
<td>On resistance P-channel</td>
<td>R_{ONP}</td>
<td>-</td>
<td>3</td>
<td>- Ω, I_{O}=20mA</td>
</tr>
</tbody>
</table>
Electrical characteristics (unless otherwise specified VIN=12V and Ta=25°C)

3. General

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Limits</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Average supply current</td>
<td>$I_{CC}$</td>
<td>-</td>
<td>5</td>
<td>8</td>
</tr>
<tr>
<td>Oscillator</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Oscillation frequency1</td>
<td>$F_{OSC1}$</td>
<td>600</td>
<td>750</td>
<td>900</td>
</tr>
<tr>
<td>Oscillation frequency2</td>
<td>$F_{OSC2}$</td>
<td>400</td>
<td>500</td>
<td>600</td>
</tr>
<tr>
<td>Protections</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Under voltage lockout threshold1</td>
<td>$V_{UVLO1}$</td>
<td>6.9</td>
<td>7.4</td>
<td>7.9</td>
</tr>
<tr>
<td>Under voltage lockout threshold2</td>
<td>$V_{UVLO2}$</td>
<td>6.5</td>
<td>7.0</td>
<td>7.5</td>
</tr>
<tr>
<td>Thermal Shutdown</td>
<td>$T_{TSD}$</td>
<td>-</td>
<td>175</td>
<td>-</td>
</tr>
<tr>
<td>Short Circuit Protection Time 1</td>
<td>$T_{SCP1}$</td>
<td>153</td>
<td>219</td>
<td>285</td>
</tr>
<tr>
<td>Short Circuit Protection Time 2</td>
<td>$T_{SCP2}$</td>
<td>230</td>
<td>328</td>
<td>426</td>
</tr>
<tr>
<td>FB threshold1 for SCP</td>
<td>$V_{FBSCP1}$</td>
<td>0.985</td>
<td>1.065</td>
<td>1.145</td>
</tr>
<tr>
<td>FB threshold2 for SCP</td>
<td>$V_{FBSCP2}$</td>
<td>-</td>
<td>0.969</td>
<td>-</td>
</tr>
<tr>
<td>FBB threshold1 for SCP</td>
<td>$V_{FBBSCP1}$</td>
<td>-</td>
<td>1.055</td>
<td>-</td>
</tr>
<tr>
<td>FBB threshold2 for SCP</td>
<td>$V_{FBBSCP2}$</td>
<td>-</td>
<td>0.874</td>
<td>-</td>
</tr>
<tr>
<td>FBP threshold1 for SCP</td>
<td>$V_{FBBSCP1}$</td>
<td>-</td>
<td>0.967</td>
<td>-</td>
</tr>
<tr>
<td>FBP threshold2 for SCP</td>
<td>$V_{FBBSCP2}$</td>
<td>-</td>
<td>0.859</td>
<td>-</td>
</tr>
<tr>
<td>FBN threshold1 for SCP</td>
<td>$V_{FBNSCP1}$</td>
<td>-</td>
<td>0.406</td>
<td>-</td>
</tr>
<tr>
<td>FBN threshold2 for SCP</td>
<td>$V_{FBNSCP2}$</td>
<td>-</td>
<td>0.505</td>
<td>-</td>
</tr>
<tr>
<td>Reference Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Voltage</td>
<td>$V_{REF}$</td>
<td>1.188</td>
<td>1.213</td>
<td>1.238</td>
</tr>
<tr>
<td>Gate Drive</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate drive threshold</td>
<td>$V_{GD}$</td>
<td>0.985</td>
<td>1.065</td>
<td>1.145</td>
</tr>
<tr>
<td>GD output low voltage</td>
<td>$V_{OL}$</td>
<td>-</td>
<td>0.7</td>
<td>1.4</td>
</tr>
<tr>
<td>GD output leakage current</td>
<td>$I_{LK}$</td>
<td>-</td>
<td>0</td>
<td>10</td>
</tr>
<tr>
<td>Logic signals EN1, EN2, FREQ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High level input voltage</td>
<td>$V_{IH}$</td>
<td>2.0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Low level input voltage</td>
<td>$V_{IL}$</td>
<td>-</td>
<td>-</td>
<td>0.8</td>
</tr>
</tbody>
</table>

* This product is not designed for protection against radioactive rays.
Reference Data (Unless otherwise specified, Ta = 25°C)

Fig.1 SUPPLY CURRENT

Fig.2 SUPPLY CURRENT

Fig.3 STANDBY CURRENT

Fig.4 REF VOLTAGE

Fig.5 SWITCHING FREQUENCY

Fig.6 SS SOURCE CURRENT

Fig.7 DLY1,2 SOURCE CURRENT

Fig.8 INPUT BIAS CURRENT

Fig.9 INPUT BIAS CURRENT

Fig.10 EN1 THRESHOLD VOLTAGE

Fig.11 EN2 THRESHOLD VOLTAGE

Fig.12 SW ON RESISTANCE
Reference Data (Unless otherwise specified, Ta = 25°C)

Fig.13 SWB ON RESISTANCE

Fig.14 DRP ON RESISTANCE

Fig.15 DRN ON RESISTANCE

Fig.16 OVP WAVEFORM

Fig.17 STEP UP EFFICIENCY

Fig.18 STEP UP EFFICIENCY

Fig.19 STEP DOWN EFFICIENCY

Fig.20 STEP DOWN EFFICIENCY

Fig.21 START UP WAVEFORM
EN1 terminal should be pulled-up to VIN terminal.

Fig.23 Typical Application
## Pin Assignment Diagram

![Pin Assignment Diagram](image)

### Pin Assignment and Pin Function

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin name</th>
<th>Function</th>
<th>Pin No.</th>
<th>Pin name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FB</td>
<td>Feedback input 1 for VS</td>
<td>15</td>
<td>FBB</td>
<td>Feedback input for Vlogic</td>
</tr>
<tr>
<td>2</td>
<td>COMP</td>
<td>Error amp output</td>
<td>16</td>
<td>EN1</td>
<td>Enable pin for Vlogic and VGL</td>
</tr>
<tr>
<td>3</td>
<td>OS</td>
<td>Output sense pin</td>
<td>17</td>
<td>BOOT</td>
<td>Capacitance connection pin for booting</td>
</tr>
<tr>
<td>4</td>
<td>SW</td>
<td>Switching pin for VS</td>
<td>18</td>
<td>SWB</td>
<td>Switching pin for Vlogic</td>
</tr>
<tr>
<td>5</td>
<td>SW</td>
<td>Switching pin for VS</td>
<td>19</td>
<td>N.C.</td>
<td>Non-connect pin</td>
</tr>
<tr>
<td>6</td>
<td>PGND</td>
<td>Ground pin</td>
<td>20</td>
<td>VINB</td>
<td>Power supply input pin</td>
</tr>
<tr>
<td>7</td>
<td>PGND</td>
<td>Ground pin</td>
<td>21</td>
<td>VINB</td>
<td>Power supply input pin</td>
</tr>
<tr>
<td>8</td>
<td>SUP</td>
<td>Power supply input pin</td>
<td>22</td>
<td>AVIN</td>
<td>Power supply input pin</td>
</tr>
<tr>
<td>9</td>
<td>EN2</td>
<td>Enable pin for VS and VGH</td>
<td>23</td>
<td>GND</td>
<td>Analog Ground pin</td>
</tr>
<tr>
<td>10</td>
<td>DRP</td>
<td>Switching pin for VGH</td>
<td>24</td>
<td>REF</td>
<td>Internal reference output pin</td>
</tr>
<tr>
<td>11</td>
<td>DRN</td>
<td>Switching pin for VGL</td>
<td>25</td>
<td>DLY1</td>
<td>Delay start capacitance connection pinfor VGL</td>
</tr>
<tr>
<td>12</td>
<td>FREQ</td>
<td>Frequency</td>
<td>26</td>
<td>DLY2</td>
<td>Delay start capacitance connection pinfor VS</td>
</tr>
<tr>
<td>13</td>
<td>FBN</td>
<td>Feedback input 1 for VGL</td>
<td>27</td>
<td>GD</td>
<td>Gate drive pin for load switch</td>
</tr>
<tr>
<td>14</td>
<td>FBP</td>
<td>Feedback input 1 for VGH</td>
<td>28</td>
<td>SS</td>
<td>Soft start capacitance connection pin for VS</td>
</tr>
</tbody>
</table>
Block Operation

- **VREG**
  A block to generate constant-voltage for DC/DC boosting.

- **VREF**
  A block that generates internal reference voltage of 2.9 V (Typ.).

- **TSD/UVLO**
  TSD (Thermal shutdown)/UVLO (Under Voltage Lockout) protection block. The TSD circuit shuts down IC at 175°C (Typ.)
  The UVLO circuit shuts down the IC when the Vcc is 7 V (Typ.) or below.

- **Error amp block (ERR)**
  This is the circuit to compare the reference voltage and the feedback voltage of output voltage. The COMP pin voltage resulting from this comparison determines the switching duty. At the time of startup, since the soft start is operated by the SS pin voltage, the COMP pin voltage is limited to the SS pin voltage.

- **Oscillator block (OSC)**
  This block generates the oscillating frequency.

- **SLOPE block**
  This block generates the triangular waveform from the clock created by OSC. Generated triangular waveform is sent to the PWM comparator.

- **PWM block**
  The COMP pin voltage output by the error amp is compared to the SLOPE block's triangular waveform to determine the switching duty. Since the switching duty is limited by the maximum duty ratio which is determined internally, it does not become 100%.

- **DRV block**
  A DC/DC driver block. A signal from the PWM is input to drive the power FETs.

- **CURRENT SENSE**
  Current flowing to the power FET is detected by voltage at the CURRENT SENSE and the overcurrent protection operates at 2.0/2.6A (min.). When the overcurrent protection operates, switching is turned OFF and the SS pin capacitance is discharged.

- **DELAY START**
  A start delay circuit for positive/negative charge pump and Boost converter.

- **Soft start circuit**
  Since the output voltage rises gradually while restricting the current at the time of startup, it is possible to prevent the output voltage overshoot or the rush current.

- **Positive charge pump**
  A controller circuit for the positive-side charge pump. The switching amplitude is controlled so that the feedback voltage FBP will be set to 1.213 V (Typ.).
  The start delay time can be set in the DLY2 pin at the time of startup. When the DLY2 voltage reaches 0.65 V (Typ.), switching waves will be output from the DRP pins.

- **Negative charge pump**
  A controller circuit for the negative-side charge pump. The switching amplitude is controlled so that the feedback voltage FBN will be set to 0.2 V (Typ.).
  The start delay time can be set in the DLY1 pin at the time of startup. When the DLY2 voltage reaches 0.65 V (Typ.), switching waves will be output from the DRN pins.

- **Over Voltage protection of the Boost Converter**
  The boost converter has an overvoltage protection to protect the internal power MOS FET (SW) in case the feed back (FB) pin is floating or shorted to GND. Vs voltage is monitored with comparator over the OS pin. When the voltage of OS pin reached 19V (typ.), the Boost Converter stops its switching until the OS pin voltage falls below the comparator threshold.
**Start-up Sequence**

The DC/DC converter of this IC incorporates a soft start function, and the charge pump incorporates a delay function, for which independent time settings are possible through external capacitors. As the capacitance, 0.01 µF to 0.1 µF is recommended. If the capacitance is set lower than 0.01 µF, the overshooting may occur on the output voltage. If the capacitance is set larger than 0.1 µF, the excessive back current flow may occur in the internal parasitic elements when the power is turned OFF and it may damage IC. When the capacitor more than 0.1 µF is used, be sure to insert a diode to VIN in series, or a bypass diode between the SS and VIN pins.

![Fig.25 Example of Bypass Diode Use](image)

When there is the activation relation (sequences) with other power supplies, be sure to use the high-precision product (such as X5R). Soft start time may vary according to the input voltage, output loads, coils, voltage, and output capacitance. Be sure to verify the operation using the actual product.

A delay of the charge pump starts from a point where \( V_{LOGIC} \) reaches 85% of its nominal value (Typ.).

- Soft start time of DC/DC converter block: \( t_{SS} \)
  \[ t_{SS} = \frac{C_{ss} \times 0.6}{10} \mu A \text{ [s]} \]
- Delay time of charge pump block: \( t_{DELAY} \)
  \[ t_{DELAY} = \frac{C_{ss} \times 0.65}{5} \mu A \text{ [s]} \]

Where, \( C_{ss} \) is an external capacitor.

![Startup example](image)

\[ t_{SS} = \frac{C_{ss} \times 0.6}{10} \mu A \text{ [s]} \]
\[ t_{DELAY} = \frac{C_{ss} \times 0.65}{5} \mu A \text{ [s]} \]

Where, \( C_{ss} \) is an external capacitor.

![Fig. 26 Output Timing Sequence with EN2 always high (EN2=VIN)](image)

![Fig. 27 Output Timing Sequence(with using EN1 and EN2)](image)
**Short Circuit Protection**

BD8160AEFV has a short circuit protection feature to prevent the large current flowing when the output is shorted to GND. This function is monitoring \( V_S \), \( V_{LOGIC} \), \( V_{GH} \) and \( V_{GL} \) voltage and starts the timer when at least one of the outputs is not operating properly (when the output voltage was lower than expected) After TBD ms (Typ) of this abnormal state, BD8160AEFV will shutdown the all outputs and latch the state.

The timer operation will be done even when BD8160AEFV starts up. Therefore, please adjust the capacitor for SS, DLY1 and DLY2 (Softstart and Delaystart) so that the all output voltage reach the expected value within the Short Circuit Protection Time (TBD ms Typ)

![Diagram](image-url)
Selecting Application Components

(1) Output LC constant (Boost Converter)

The inductance L to use for output is decided by the rated current ILR and input current maximum value IOMAX of the inductance.

Adjust so that IOMAX + ∆IL does not reach the rated current value ILR. At this time, ∆IL can be obtained by the following equation.

$$\Delta IL = \frac{1}{L} \times \frac{V_{cc} \times (V_{o} - V_{cc})}{V_{o}} \times \frac{1}{f} [A]$$

Set with sufficient margin because the inductance L value may have the dispersion of ± 30%.

For the capacitor C to use for the output, select the capacitor which has the larger value in the ripple voltage VPP permissible value and the drop voltage permissible value at the time of sudden load change.

Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = I_{OMAX} \times \frac{1}{fC_{o}} \times \frac{V_{cc} \times (I_{OMAX} - \frac{\Delta IL}{2})}{V_{o}} [V]$$

Perform setting so that the voltage is within the permissible ripple voltage range.

For the drop voltage VDR during sudden load change, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I}{C_{o}} \times 10 \mu s [V]$$

However, 10 µs is the rough calculation value of the DC/DC response speed.

Make Co settings so that these two values will be within the limit values.

(2) Output LC constant (Buck Converter)

The inductance L to use for output is decided by the rated current ILR and input current maximum value IOMAX of the inductance.

Adjust so that IOMAX + ∆IL does not reach the rated current value ILR. At this time, ∆IL can be obtained by the following equation.

$$\Delta IL = \frac{1}{L} \times \frac{V_{cc} \times (V_{o} - V_{cc})}{V_{o}} \times \frac{1}{f} [A]$$

Set with sufficient margin because the inductance L value may have the dispersion of ± 30%.

For the capacitor C to use for the output, select the capacitor which has the larger value in the ripple voltage VPP permissible value and the drop voltage permissible value at the time of sudden load change.

Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = \frac{\Delta IL \times RESR + \Delta IL \times V_{o}}{2C_{o} \times V_{cc} \times \frac{1}{f}} [V]$$

Perform setting so that the voltage is within the permissible ripple voltage range.

For the drop voltage VDR during sudden load change, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I}{C_{o}} \times 10 \mu s [V]$$

However, 10 µs is the rough calculation value of the DC/DC response speed.

Make Co settings so that these two values will be within the limit values.
(3) Phase compensation  
Phase Setting Method  
The following conditions are required in order to ensure the stability of the negative feedback circuit.

- Phase lag should be 150° or lower during gain 1 (0 dB) (phase margin of 30° or higher).

Because DC/DC converter applications are sampled using the switching frequency, the overall GBW should be set to 1/10 the switching frequency or lower. The target application characteristics can be summarized as follows:

- Phase lag should be 150° or lower during gain 1 (0 dB) (phase margin of 30° or higher).
- The GBW at that time (i.e., the frequency of a 0-dB gain) is 1/10 of the switching frequency or below.

In other words, because the response is determined by the GBW limitation, it is necessary to use higher switching frequencies to raise response.

One way to maintain stability through phase compensation involves canceling the secondary phase lag (-180°) caused by LC resonance with a secondary phase advance (by inserting 2 phase advances).

The GBW (i.e., the frequency with the gain set to 1) is determined by the phase compensation capacitance connected to the error amp. Increase the capacitance if a GBW reduction is required.

(a) Standard integrator (low-pass filter)  
(b) Open loop characteristics of integrator

![Fig. 33](image1)  
![Fig. 34](image2)

Point (a) \( f_a = \frac{1}{2\pi RA} \) [Hz]  
Point (b) \( f_b = \text{GBW} = \frac{1}{2\pi RC} \) [Hz]

The error amp performs phase compensation of types (a) and (b), making it act as a low-pass filter.

For DC/DC converter applications, R refers to feedback resistors connected in parallel.

From the LC resonance of output, the number of phase advances to be inserted is two.

![Fig. 35](image3)

LC resonant frequency \( f_p = \frac{1}{2\pi \sqrt{LC}} \) [Hz]  
Phase advance \( f_{z1} = \frac{1}{2\pi C_1R_1} \) [Hz]  
Phase advance \( f_{z2} = \frac{1}{2\pi C_2R_3} \) [Hz]

Set a phase advancing frequency close to the LC resonant frequency for the purpose of canceling the LC resonance.
(4) Design of Feedback Resistance constant
Set the feedback resistance as shown below.

\[ V_s, V_{\text{LOGIC}} = \frac{R_1 + R_2}{R_2} \times \text{Reference Voltage} \ [V] \]

(5) Positive-side Charge Pump Settings
The IC incorporates a charge pump controller, thus making it possible to generate stable gate voltage.
The output voltage is determined by the following equation. As the setting range, 10kΩ to 330kΩ is recommended. If the resistor is set lower than 10kΩ, it causes reduction of power efficiency. If it is set more than 330kΩ, the offset voltage becomes larger by the input bias current of 0.1µA (Typ.) in the internal error amp.

\[ \text{Vo2} = \frac{R_6 + R_7}{R_7} \times \text{Reference Voltage} \ [V] \]

By connecting capacitance to the DLY2 pin, the rising delay time can be set for the positive-side charge pump output. The delay time is determined by the following equation.

- Delay time of charge pump block \( t_{\text{DELAY}} \)
  \[ t_{\text{DELAY}} = \frac{(C_{\text{DLS}} \times 0.65)}{5 \mu A \ [s]} \]
  Where, \( C_{\text{DLS}} \) is an external capacitor.

(6) Negative-side Charge Pump Settings
BD8160AEFV incorporates a charge pump controller for negative voltage, thus making it possible to generate stable gate voltage.
The output voltage is determined by the following equation. As the setting range, 10kΩ to 330kΩ is recommended. If the resistor is set lower than 10kΩ, it causes reduction of power efficiency. If it is set more than 330kΩ, the offset voltage becomes larger by the input bias current of 0.1µA (Typ.) in the internal error amp.

\[ V_{\text{GL}} = - \frac{R_8}{R_9} \times 1.013 + 0.2 \ [V] \]

Like the positive-side charge pump, the rise delay time can be set by connecting capacitance to the DLY1 pin.
Selecting the Feedforward Capacitor (Boost Converter)
Across the upper resistor $R_1$, a bypass capacitor is needed to have a stable converter loop. $C_1$ will set a zero in the loop together with $R_1$.

![C1 and R1 diagram](image)

$$C_1 = \frac{1}{2\pi \times f_{Z1} \times R_1}$$

$F_{Z1} = 11\text{kHz}$

Fig.39

The regulator loop can be compensated by adjusting the external components connected to the COMP pin. $C_2, R_2$ are decided by the following formula.

$$F_{Z1} = 11\text{kHz} = \frac{1}{2\pi \times C_2 \times R_2}$$

Selecting the Feedforward Capacitor (Buck converter)
The feedforward capacitor across the upper feedback resistor divider sets a zero in the control loop.

![C3 and R3 diagram](image)

$$C_3 = \frac{1}{2\pi \times f_{Z2} \times R_3}$$

$F_{Z2} = 12\text{kHz}$

Fig.40
### I/O Equivalent Circuit Diagram

<table>
<thead>
<tr>
<th>18.SWB</th>
<th>17.BOOT</th>
<th>25.DLY1 26.DLY2 28.SS</th>
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<table>
<thead>
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<th>3.OS</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image10" alt="I/O Circuit" /></td>
</tr>
</tbody>
</table>

Fig.41
Notes for use

1) Absolute maximum ratings
   Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential
   Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat
   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting
   Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field
   Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards
   When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns
   When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) Regarding input pin of the IC
   This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when the resistors and transistors are connected to the pins as shown in Fig.42, a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage. The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.

9) Overcurrent protection circuits
   An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

10) Thermal shutdown circuit (TSD)
    This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature $T_j$ will trigger the TSD circuit to turn off all output power elements. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

11) Testing on application boards
    At the time of inspection of the installation boards, when the capacitor is connected to the pin with low impedance, be sure to discharge electricity per process because it may load stresses to the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

12) EN1 terminal
    EN1 terminal should be pulled up to VIN terminal.
Power Dissipation

On 70 × 70 × 1.6 mm glass epoxy PCB
(1) 1-layer board (Backside copper foil area 0 mm × 0 mm)
(2) 2-layer board (Backside copper foil area 15 mm × 15 mm)
(3) 2-layer board (Backside copper foil area 70 mm × 70 mm)
(4) 4-layer board (Backside copper foil area 70 mm × 70 mm)
Ordering part number

B D 8 1 6 0 A E F V - E 2

Part No. Part No. Package Packaging and forming specification

EFV: HTSSOP-B28 E2: Embossed tape and reel

HTSSOP-B28

Tape and Reel information

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<thead>
<tr>
<th>Tape</th>
<th>Embossed carrier tape (with dry pack)</th>
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</thead>
<tbody>
<tr>
<td>Quantity</td>
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</tr>
<tr>
<td>Direction of feed</td>
<td>E2</td>
</tr>
</tbody>
</table>

*Order quantity needs to be multiple of the minimum quantity.*
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1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM’s Products for Specific Applications.

(Note 1) Medical Equipment Classification of the Specific Applications

<table>
<thead>
<tr>
<th>JAPAN</th>
<th>USA</th>
<th>EU</th>
<th>CHINA</th>
</tr>
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<tr>
<td>CLASS III</td>
<td>CLASS III</td>
<td>CLASS II b</td>
<td>CLASS III</td>
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</tbody>
</table>

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:

[a] Installation of protection circuits or other protective devices to improve system safety
[b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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[b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
[c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
[d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
[e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
[f] Sealing or coating our Products with resin or other coating materials
[g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
[h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification
Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM’s internal use only.

Precaution for Disposition

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